The use of nanowires for the production of a power Schottky diode

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Author's Declaration

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Signature of Author: 

Keith Brian McGrath

Leicester, April 2018

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Abstract

The reduction in carbon emissions targets of 2050 are challenging and require a number of diverse ways, and probably yet to be invented methods, to reduce the worlds energy consumption. Therefore more energy efficient electrical and electronic devices, and equipment, can play a major role in this. Although their individual contribution is small, due to their mass scale, they should be able to contribute significantly.

This research has been aimed at producing such a device, a Schottky diode, which has been constructed in such a manner that it will be more energy efficient than a similar device made the traditional way, using the principle of surface area to volume ratio.

The Schottky diode has a characteristic that the current through the device increases with an increase in temperature, in both the forward and reverse biased directions. This leads to the device being less efficient, and energy consumption is increased to no benefit of the circuit it is used in.

Two types of devices have been constructed, one from small diameter Si pillars, and the other type from a single large diameter pillar. Both devices are designed to have the same volume of Si, but the devices constructed from the small diameter pillars will have a higher surface area to volume ratio. The devices with the higher surface area to volume ratio will operate at a lower temperature for the same voltage, current and power dissipated.

This research has demonstrated that if the devices are made from the pillars, they will have a lower operating temperature, and hence will be a more energy efficient device.

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List of Acronyms

Bi……..…Biot Number

Csv……Comma Separated Variable

CVD…….….Chemical Vapour Deposition

DMU……De Montfort University

GPIB……..……....General Purpose Interface Bus

I…….……Current

IPA……..…….Isopropyl Alcohol

I-V…….……Current – Voltage

I-V-T……Current-Voltage-Temperature

HP……..……Hewlett Packard

KOH……..……Potassium Hydroxide

MOCVD……..…….Metalorganic Chemical Vapour Deposition

PC……..Personal Computer

PECVD…….……..……Plasma Enhanced Chemical Vapour Deposition

PT100……..…….Platinum Resistance Temperature Device

R…….…….Resistance

RI……..Refractive Index

RIE……..……Reactive Ion Etching

RF…….……Radio Frequency

rpm……..…….Revolutions per Minute

RTD…..……..Resistance Temperature Device

sccm…….…..…..…..Standard Cubic Centimetre per Minute

SEM…….....Scanning Electron Microscope

Si……..Silicon

SiNW…….……..Silicon Nanowires

SiNx…….……...……Silicon Nitride

UV……Ultra Violet

Vdc.…….….Direct Current Voltage

VLS……...……Vapour/Liquid/Solid

VLSI……..……Very Large Scale Integration

°C……Degrees Celsius

Chapter 1 **Introduction**

This section of my thesis gives an overview of my research, the objectives of the research, the organisation of the thesis and a summary of the outcomes of my research.

1.1 **Research Overview**

The intention at the start of my research was to construct a power Schottky diode from nanowires, then test this device, and compare this with a traditionally constructed bulk Si Schottky diode, to see if a more energy efficient (less wasted energy in the form of heat) diode could be constructed by reducing the operating temperature. Utilising the properties of nanowires and the increased surface area to volume ratio which would be achieved. The reduced temperature would also have the benefit of increasing the diode life span. The nanowires were to be grown at DMU by another student and I was to utilise these for constructing my Schottky diodes. The production of vertical nanowires has proved very difficult and it was envisaged that these would not be ready in time for my research. An alternative strategy was developed to produce Schottky diodes, with a top down process, and a pillar range of 30 to 50 μm in diameter. To demonstrate the reduced operating temperature of the new diodes compared to those of a solid construction, with the anticipation that the operating temperature of the new style diodes would be less than those of solid construction for an identical power dissipation, thus concluding that the new style diodes were more energy efficient.

My research has investigated the Schottky diode, and the heating up and cooling down of such devices. A Schottky diode is an electronic component which is used for its fast forward biased switch on time, and its low reverse biased leakage current, and is widely used for example in switch mode power supplies.

The Schottky diode does have some undesirable characteristics, one of those being temperature. Si Schottky diodes have a maximum operating temperature that once breached, the Schottky barrier will breakdown, and will not recover and renders the device useless. This is quite a high temperature in the range of 100

to 200 °C and correct selection of the Schottky diode for its intended use should avoid any issues with this temperature limit. There is also the fact that when a Schottky diode is drawing current, the device will heat up, as with most electronic devices. This rise in temperature also increases the current being drawn. This will not lead to thermal runaway but does mean that as the Schottky diode heats up the current rises, and the Schottky diodes energy efficiency decreases, with increased power dissipation, and no benefit to the circuit it is being used in. In addition reliability of the diodes is reduced, with increased operating temperature.

The research has investigated the heating effects of the Schottky diode, and a way of reducing the power being used by the Schottky diode, by reducing the increase in the current being drawn by the Schottky diode as it heats up. This will be by the well-known theorem of the ratio of surface area to volume as discussed in the next chapter.

In simple terms my research has focused on producing a Schottky diode with more surface area to volume ratio than a standard bulk Schottky diode, by constructing the device from pillars. For comparison purposes two types of Schottky diodes will be constructed, ones with a solid construction and ones constructed with pillars, with the two types having the same volume.

1.2 Organisation of thesis

The thesis is divided into 10 Sections describing the background, etching techniques, device construction, measurement / characteristic techniques and testing. Following this chapter which gives an overview of the research the thesis is organised as detailed below.

Chapter 2 – This chapter gives some background information with regard to heat transfer and the literature searches which have been carried out to complement the research. The heat transfer section is important as this gives theoretical information for which to compare the results obtained.

Chapter 3 – This chapter describes the electrical characteristic measurements performed on the Schottky diodes, with an overview of the characteristic and how this has been used.

Chapter 4 – This chapter details all of the physical characteristic techniques which have been employed during my research, it gives an overview of the technique and then how this has been used in my research.

Chapter 5 – This chapter investigates the heat transfer characteristics of the Schottky diodes and includes the technique which has been developed and how this relates to heat transfer theory of chapter 2.

Chapter 6 – This chapter is devoted to CF_4 etching of Si which has been carried out, with trials carried out to ascertain the etch rate which would be possible with 100% CF_4, and some tests carried out on some Schottky diodes constructed by this method.

Chapter 7 – This chapter looks at the etching that has been carried out by potassium hydroxide (KOH) and the optimisation of this.

Chapter 8 – This chapter investigates the manufacturing of the Schottky Diodes and the processes that have been carried out to fabricate them, together with the equipment used in the fabrication.

Chapter 9 – This chapter describes the electrical and temperature characteristics and the results that have been achieved.

Chapter 10 – This chapter concludes my research and looks at possible future scope for the continued research in this area.

1.3 Summary of the outcomes

In summary of the research carried out, two types of Schottky diodes have been produced, one of a more traditional construction being made from solid Si and the other type of pillar construction. Electrical characteristic measurements have been carried out to ascertain the quality of the diodes produced, and surface temperature measurements have been carried out to ascertain the energy efficiency.

The surface temperature measurements have been used as a comparison of the two types of diodes, in anticipation that these would demonstrate that the diode constructed from pillars, which has a higher surface area to volume ratio would

ultimately operate at a lower temperature, and therefore be more energy efficient, due to the fact that a temperature increase in the diode will produce a rise in the current, at no benefit to the circuit it is used in.

My research has concluded that the diodes made from the pillar construction will operate at a lower temperature and hence will be more energy efficient.

My research has increased the knowledge around CF_4 etching and with the production of a Schottky diode with a pillar construction using this method, which shows good electrical characteristics.

In addition, a method to carry out temperature measurements has been developed, to demonstrate that the devices that are constructed from pillars have a lower operating temperature, and hence will be more energy efficient.

Chapter 2 **Literature Review**

2.1 Introduction

This section of the thesis gives details of the background research and literature reviews which have been carried out, as part of the research, to give the reader an understanding of the basis on which the research has been based.

2.2 Energy Consumption

The reduction in energy consumption and the need to produce energy from renewable sources, to reduce the worldwide carbon emissions, has been in the news for many years, and will be for more to come until the situation has come under control. Electronic equipment, i.e. mobile phones, computers etc. dissipate the energy / power used in the form of heat. This dissipated heat is wasted energy and gives no benefit to the equipment. In fact, as electronic devices heat up they become less energy efficient and dissipate more heat. Freescale semiconductor [1] states that a power MOSFET's on resistance increases by 70 – 100% as the temperature increases from 25°C to 150°C, which in turn increases the power dissipation with no benefit to the circuit, and hence wasted energy. There is an increasing number of electronics equipment in the world which all consume a considerable amount of energy. With this energy use, Pop [2] states that the IT infrastructure in the USA consumes in excess of 20GW, 5-10% of the national electricity budget. Methods of reducing this wasted heat dissipation will have an effect on the energy consumption of this electronic equipment.

2.3 Heat Dissipation

The reduction of operating temperatures in electronics equipment is self-evident, with the use of heat sinks and fans in Personal Computers (PCs) and laptops. Figure 2-1 below shows a typical CPU heat sink used, and the higher the processing speed the more cooling required [2]. Incropera et al [3] states that the cumulative energy consumed worldwide to produce heat sinks is estimated to be 10^9 kW h per year. In addition, temperature also affects the life of semiconductor products and the following relationship (Equation 2-1) between life of the product and temperature is provided by Panasonic [4].

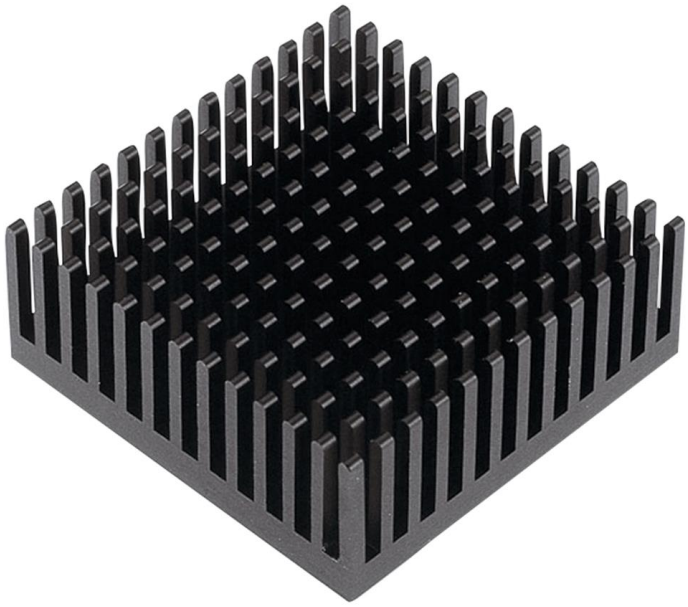

Figure 2-1 - CPU Heat Sink[1]

$$L = A\ exp\left(\frac{E_a}{kT}\right) \qquad \textbf{Equation 2-1}$$

Where;

L is the lifetime

T is the temperature (K)

A is the pre-exponential factor, a constant for each chemical reaction

E_a is the activation energy (eV)

k is the Boltzmann Constant (8.6 x 10^{-5} eV/K)

As can be seen the life of the device will be shortened as the temperature increases, with the device lifetime doubling for every 10°C decrease [5].

For the reasons stated above production methods are required to reduce the operating temperatures of electronic products, (e.g. by natural convection) by

[1] Reproduced by kind permission of RS Components

increasing the surface area to volume ratio, to reduce the wasted energy and prolong the life of the equipment.

The surface area to volume ratio is not a new theorem, but a long established one which nature has used to good effect over time. Joel Asaph Allen in 1877 formulated an ecogeographical rule “Allens’s Rule” [6], where the principle being that the volume to surface area ratio of an object determines how quickly an object can dissipate the heat within it, the higher the surface area to volume ratio the quicker the heat is dissipated. This can be seen in nature with the Inuit and Maasai tribes and their body geometry. The Inuit's live in a cold climate and need to retain heat so their surface area to volume ratio is low, and the Maasai live in a hot climate and need to lose heat so their surface area to volume ratio is high, to keep their body temperatures stable. Figure 2-2 below highlights the ability of nature.

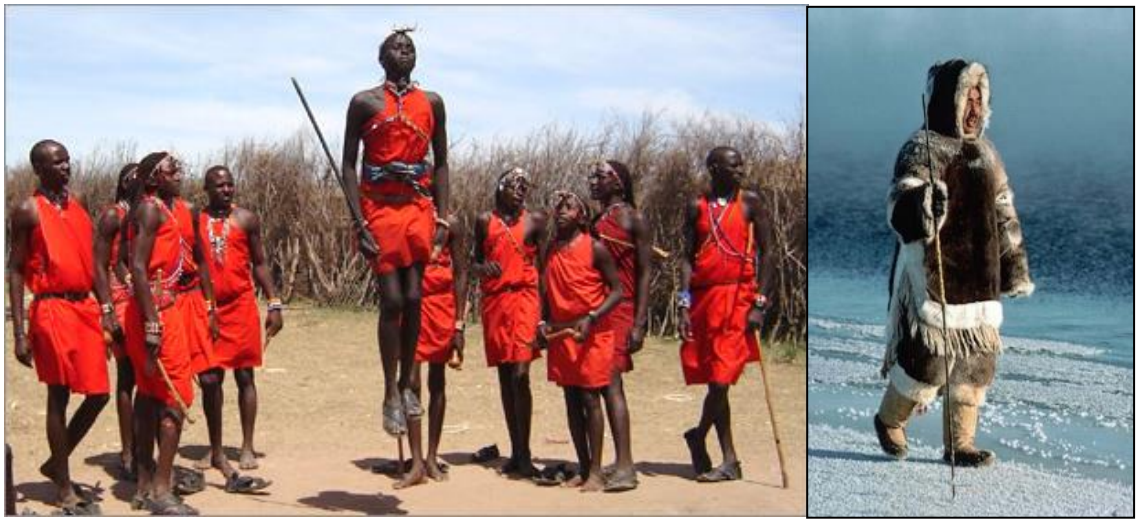

Figure 2-2 - Maasai and Inuits[2]

Another example of this is cheese cube physics by Planinsic & Vollmer [7] where different sized cheese cubes are heated up firstly in a pre-heated oven, where the smaller cubes melt first due to their internal temperature rising faster due to their small size, and secondly in a microwave oven with the results being the larger cubes melted first, owing to the simultaneous heating and cooling of the smaller cubes did not allow the cheese to rise above its melting point. This paper

[2] Reproduced by kind permission of africaupdates.com (Maasai) and Star-name-registry.com (Inuits)

then goes further to relate this to animal metabolism, animals eat food to generate body heat, assuming they all eat food in proportion to their mass, smaller animals need to eat more to keep their body temperature stable.

From the above examples it is demonstrated that the smaller the object the surface area to volume ratio is higher and the object will heat up quicker, but also cool down quicker, and will not reach the same ultimate temperature due to the simultaneous heating and cooling effect.

If for comparison reasons two different objects were constructed such that they had the same volume, but one had a higher surface area to volume ratio by constructing it from a number of smaller blocks, for the same power being dissipated through the objects the object made from multiple blocks would heat up and cool down quicker, and would not reach the same ultimate temperature.

The research will be based on a Schottky diode constructed from pillars and look into the heat dissipation as a function of surface area to volume ratio.

2.4 Schottky Diode

The power Schottky diode is an electronic component which is widely used in computers as a part of the switched mode power supply. For its fast switching speeds and its low forward biased turn on voltage, due to these being majority carrier devices. However, in achieving these characteristics, the Schottky diodes do have some disadvantages. These being;

a. A high reverse leakage current [1]
b. An increase in reverse and forward current as the temperature increases [1][8][9][10][11][12][13]
c. A relatively low reverse voltage breakdown, 100V to 200V [14]

Figure 2-3 below shows a basic diagram of a Schottky diode, which consists of a doped semiconductor, rectifying contact and an ohmic contact. Simplicity of the device does mean that they are relatively easy to construct.

The Schottky diode exhibits a rectifying behaviour, when forward biased the diode will conduct and when reverse biased only a small conduction takes place, called the reverse leakage current.

There are two types of semiconductor doping that can be used p-type or n-type, for Si, p-type is usually Boron and n-type is usually Phosphorus. P-type is so called because the majority carriers are holes where as for n-type the majority carriers are electrons. Because electrons have a higher mobility than holes [15] the n-type Schottky diode will have a faster switching speed.

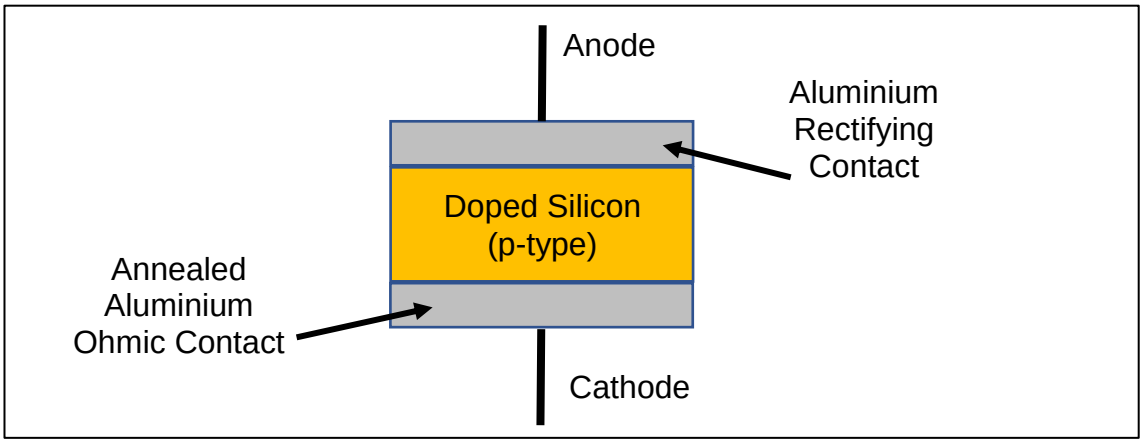

Figure 2-3 - Basic Schottky diode diagram

The rectifying contact is formed when a metal, that has a lower work function than the semiconductor, are placed in contact with each other. This forms a barrier, where the height of this is approximately the midpoint between the metal and semiconductor work functions [15]. The barrier formed stops conduction in the reversed biased condition and allows conduction in the forward biased condition, once the barrier has been overcome with a high enough potential, this potential being the turn on voltage. Sze et al [15] provides a graph of typical metal work functions, the typical rectifying contact used for Si is Al.

The ohmic contact needs to provide a low resistance contact with respect to the semiconductor, so that the charge carriers can flow in and out of the diode with ease. The typical ohmic contact for Si is Al [15] this is evaporated onto the surface of the Si and then annealed at the Al eutectic temperature of 450 °C, this diffuses the Si and Al and creates a low resistance contact.

From point b. above, the current rises as the temperature of the diode increases, this can be seen from the Schottky diode current equation presented by Sze et al [15], Equation 2-2 below.

$$J = A^{**}T^2 exp\left(\frac{-q\emptyset_{Bn}}{kT}\right)\left[exp\left(\frac{qV}{kT}\right) - 1\right]$$ **Equation 2-2**

Where;

J = Diode current (A)

A^{**} = Effective Richardson Constant (A/cm^2-K^2)

T = Temperature (K)

q = Electronic Charge (C) 1.6E^{-19}

$\emptyset_{Bn}$ = Barrier Height (V)

k = Boltzmann's Constant (J/K) 1.38E^{-23}

V = Bias Voltage (V)

To show the temperature-current relationship the following values have been entered into Equation 2-2 for a temperature range of 298-350 K, and are shown in graphs Figure 2-4 for forward biased with a voltage of 0.7V and Figure 2-5 for reversed biased with a voltage of -0.7V.

A^{**} = 120 A/cm^2-K^2, q = 1.6E^{-19} C, $\emptyset_{Bn}$ = 1.12 V, k = 1.38E^{-23} J/K, V = 0.7 V or -0.7 V.

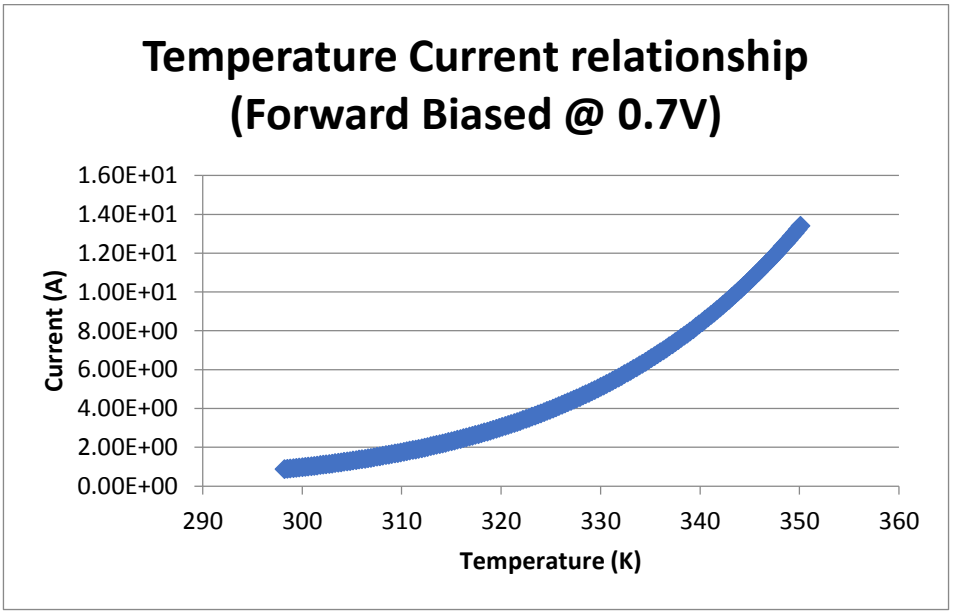

Figure 2-4 - Calculated temperature current relationship (forward biased @ 0.7V)

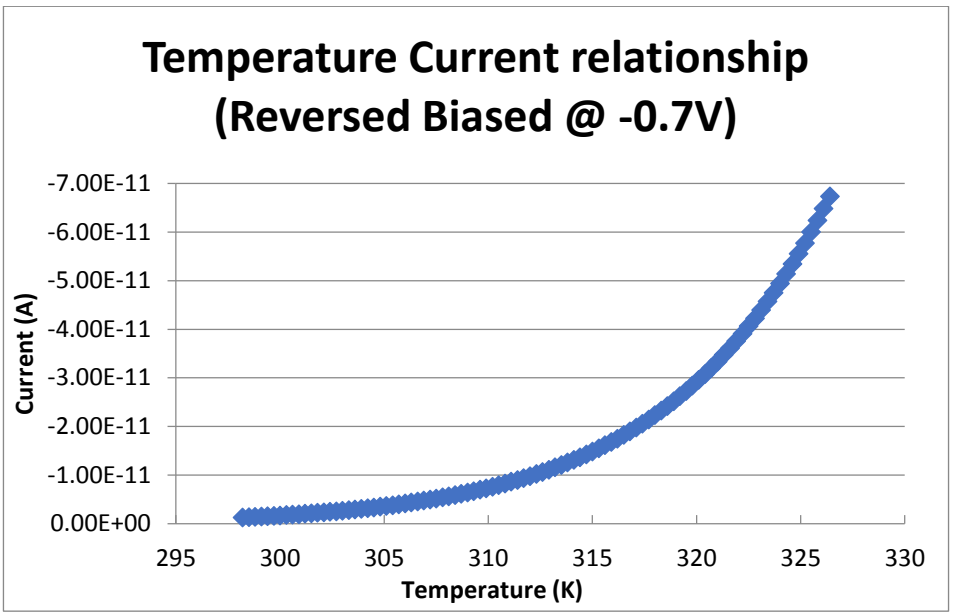

Figure 2-5 - Calculated temperature current relationship (reversed biased @ -0.7V)

In addition, a simple test has been carried out on a Schottky diode by heating the diode up on a hot plate and recording the I-V measurements, the test has been carried out over a temperature range of room temperature to 70°C, Figure 2-6 below shows the graph of the currents and it can clearly be seen that the currents in forward and reversed biased conditions increase as the temperature increases. This temperature test was carried out on a Schottky diode constructed as part of this research, SD3-2, which is a Schottky diode of solid construction.

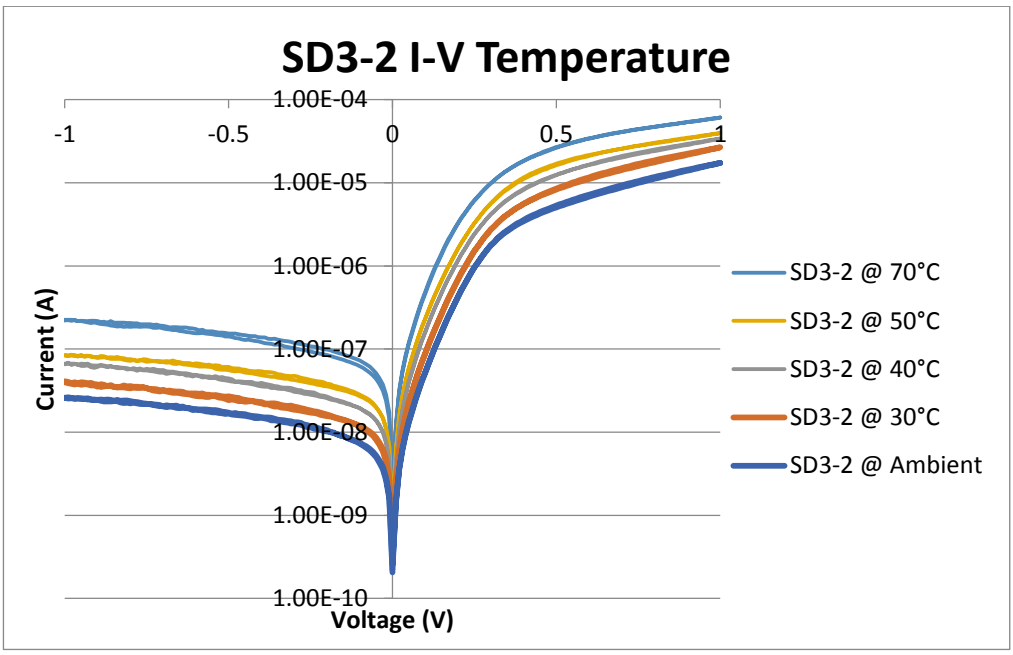

Figure 2-6 - SD3-3 Measured I-V temperature at various temperatures

As discussed above the increase in current due to temperature rise is wasted energy, and a different way of producing these diodes is required to ensure that they will operate at a lower temperature by natural heat convection.

This could be achieved by producing the diodes with a multiple pillar construction with micro / nanowires rather than the traditional way out of a solid (bulk).

2.5 Nanowires

There has been a lot of research over the past years on Si nanowires and a lot has been reported on them, mainly in the field of optoelectronics sensors [16][17][18][19], gas sensors [20][21], solar cells [22][23], and those made from other material rather than Si i.e. Zinc oxide (ZnO) or Gallium Arsenide (GaN) [24] to [44], in addition there has been research on the characteristics of nanowires, Kubo et al [45] & Hafez et al [46] have looked at the current density, and concludes that this increases as the width of the nanowires reduces, ZhengZheng et al [47] & Piscatora et al [48], concludes that the Schottky barrier thickness decreases as the diameter decreases which gives a large ideality factor, Liu et al [49] has constructed vertical nanowires in alumina pores with good I-V characteristics, but*, not much on the production of a Si diode made from an array of Si nanowires for the sole purpose of using it as a power Schottky diode, and*

no research papers could be found on measuring the temperature of Schottky diodes made from pillar construction.

There are examples of temperature analysis being carried out on single nanowires, Sachet et al [50] looks at the thermal conductance, and concludes that the thermal conductance increases in nanowires with a larger surface area to volume ratio. Pop et al [51] has looked at the thermal conductivity, and suggested that a 10nm thin Si film is expected to have a thermal conductivity of one order of magnitude less than that of bulk Si. Pop et al [52], which is very similar to his work presented in [51], indicating that there is not much research on the thermal conductivity of nanowires. Hasan et al [53] has looked at nanopyramids, and the photothermal response of those. Research carried out so far shows thermal conductivity of nanowires is less than bulk Si, this would be of concern if just using a single nanowire since the heat dissipation would be slower than bulk Si, however, if using a forest of nanowires, and assuming the power would be distributed equal amongst them, the total heat dissipation should be greater, according to Equation 2-3.

$$k_B < \frac{D_B}{D_{NW}} \times k_{NW} \qquad \textbf{Equation 2-3}$$

Where;

k_B = Thermal conductivity of bulk ($Wm^{-1}\ K^{-1}$)

D_B = Diameter of Bulk (m)

D_{NW} = Diameter of the nanowire (m)

k_{NW} = Thermal conductivity of the nanowire ($Wm^{-1}\ K^{-1}$)

As an example, from [51] k_B = 148 ($Wm^{-1}\ K^{-1}$), from [2] k_{NW} for 10nm = 10 ($Wm^{-1}\ K^{-1}$), therefore D_{NW} = $10x10^{-9}$ and D_B = $1x10^{-3}$ (1mm) Equation 2-3 equates to;

$$148 < \frac{1 \times 10^{-3}}{10 \times 10^{-9}} \times 10 = 1 \times 10^{6}\ Wm^{-1}\ K^{-1}$$

In addition to the thermal characteristics of single nanowires, there is some work in the literature on Schottky diodes which have been made from nanowires, but these have been limited to mainly creating a Schottky diode with one wire [54-61], and the wire on its side with the contact deposited over the wire. However, Chang et al [62] has details of high density Si nanowires and the application in a heterojunction diode. GaN Nanowire Schottky Barrier Diodes is presented by Sabuie et al [63], and on the fabrication of metal contacts on a Si nanowire forest is detailed by Dimaggio et al [64], which also describes a method of producing the nanowires of several tens of micro meters in depth, using metal assisted chemical etching in a solution of HF (Hydrogen Fluoride), and also states that more work is required in this area.

Although, some of the papers are not based on pillar Schottky diodes, the properties of Si nanowires are discussed, which is relevant to the study presented in this thesis.

Jee et al [65] & Sheu et al [66] show that Si nanowires can be grown, and that they do have a good rectifying behaviour with low reverse current, along with Peng et al [23] & Chuah et al [27] which have shown a good rectifying behaviour. There have been mixed results with regard the ideality factor of the nanowires Heo et al [25] reports an ideality factor of 1.1 on a single nanowire Schottky diode, Park et al [26] reports ideality factors of 7 to 9, and suggests that the nanowires do not follow the normal Schottky diode equations, Bano et al [28] is reporting ideality factors of 3 to 4, which are due to the different current transport processes, Ning et al [55] with an ideality factor of 4.6, Pop et al [52] with an ideality factor of between 12 and 30, and so on, which would give an ideality factor range of 1.1 to 30. There can be a number of factors which effect the ideality factor, which are usually down to the way it which the devices have been manufactured, by having interfacial layers and surface states, which can be caused by unwanted oxide layers and material defects, which tend to lead to a high series resistance.

Sabui et al [63] discusses a concept to provide a GaN Schottky barrier diode made from an array of nanowires, through simulation, and has carried out some preliminary experiments.

Nanowires do have some interesting features, Ho et al [67] states that as nanowires are reduced in size the current density and the tunnelling component increase, and the effective barrier height reduces, which leads to a less resistive ohmic contact. Ho et al [67] and Sun et al [54] have reported that the band gap increases as the diameter of the nanowire is reduced, which will improve the breakdown voltage of the Schottky diodes.

2.6 Nanowire Construction

There are two basic ways of producing Si nanowires, either from a bottom up approach by growing the nanowires or from a top down approach by etching away the Si.

2.6.1 Bottom Up Nanowires

The most used ways of producing nanowires are from Metal Organic Chemical Vapour Deposition (MOCVD) [38][59][41], or Vapour/Liquid/Solid (VLS) [65][29] processes, using a metal catalyst, which needs to be carried out at high temperatures [28], and usually in a Plasma Enhanced Chemical Vapour Deposition (PECVD) machine.

The bottom up method of producing nanowires will not be used in this research.

2.6.2 Top Down Nanowires

Top down nanowires are produced by etching away the bulk material, in defined patterns to produce the size of nanowire required (by dry or wet etch or plasma etch).

Plasma etching is carried out in PECVD or by Reactive Ion Etching (RIE) equipment, this is performed using a discharge in a reactive gas, to create reactive atoms and radical species, that will react with the surface to form volatile compounds, which will be evaporated from the surface, thus creating the required features [68]. To form the nanowires a mask needs to be placed on the surface. The gases used are dependent on the material to be etched, for Si this is usually

SF_6 or CF_4 [68][69] as the main gas, and usually mixed with other gases like O or Cl to enhance the process. RIE is a two-part process of chemical reaction and physical bombardment, to etch Si a gas containing F is required [68] this causes a chemical reaction on the surface and creates the radicals, these are then dislodged from the surface by the ion bombardment. Dry etching allows anisotropic etch profiles to be produced as reported by Cotler et al [70]. An anisotropic etch is one that proceeds faster in one direction, more than the other directions, and is defined as the ratio of the vertical to horizontal etching rate. Anisotropic etching allows deep vertical etching to be achieved with hardly any undercutting of the mask.

Wet chemical etching does not require any expensive equipment to carry out, just a heated ultrasonic bath. The chemical of choice for etching Si is potassium hydroxide (KOH) this is mixed with H_2O of various concentrations and heated up to give the required etching speed. The samples are submerged in a solution for the required time to achieve the etch depth required, with a mask which defines the features to be etched. This method also allows anisotropic profiles but is subject to more under cutting of the mask. It can be used to produce nanostructures but there are restrictions on how close the features can be and the height of the features.

Plasma etching in CF_4 gas has been used in this research due to SF_6 not being available, and CF_4 is a much safer gas to use, this is discussed in more detail in chapter 6, wet chemical etching has also been used in this research and is discussed in more detail in chapter 7.

2.7 Heat Transfer

2.7.1 Introduction

The dissipation of heat has always been required on power semiconductor devices, and the method that has mainly been used is the use of heat sinks [71], and sometimes with the aid of a fan. Extensive literature is available on this subject, for example, Kou et al [72] which looks at the optimum fin length of heat sinks, Uppuluri [73] has looked at thermal resistance data, which is required for the sizing of heat sinks, and Mohan et al [14] looks at the component temperature

control and heat sinks. Freescale Semiconductor [1] suggests ways of optimizing the thermal environment, and one of these is to increase the surface area available for the heat to exit.

This section aims to provide information with regard to heat transfer theory, the Biot number, heating time constant and surface temperatures of two Schottky diodes, with the same volume but with different surface areas. Devices with a higher surface area to volume ratio will dissipate heat better, and to propose a suitable way that could be employed, to confirm that the diodes that have been produced with the higher surface area to volume ratio, do exhibit a better heat dissipation characteristic.

2.7.2 Heat Transfer Modes

Heat transfer can be divided into three different phases or modes, these being;

- Conduction
    - Transient
- Convection
- Radiation

2.7.2.1 Conduction

Conduction is the passage of heat through an object, this could be by having a temperature difference between two surfaces of the object, and heat would travel from the higher temperature side to the lower one through the object, or it could be from temperature derived within the object, such as chemical reactions or electrical I^2R losses (Power), or a combination of the two.

For electronic devices these usually start at ambient temperature, and as such there will be no heat transfer into the devices. Any heat generated will be internal to the devices, and will be as a consequence of the electrical current passing through the device, and so the heat transfer will be from the device to the surrounding air. It will also be assumed that the heat transfer through the device will be simple (see Biot Number below) and a constant gradient. This will mean that a more simplified method of analysis can be used, and called the lumped capacitance analysis, which is valid when the Biot number is much less than 1.

2.7.2.2 **Transient Conduction**

To account for time dependent conduction, which is usually the case where current will be applied for a short duration and the temperature measured, transient conduction needs to be considered, and the lumped capacitance method shall be used.

From Incropera et al [3] the time (t) required for a solid object to reach a certain temperature is represented by;

$$t = \frac{\rho V c}{h A_S} \ln \frac{\theta_i}{\theta} \qquad \textbf{Equation 2-4}$$

Where;

$\rho = Mass\ Density\ (Kg\ /\ m^3)\ 2330 for\ Si$

$V = The\ volume\ (m^3)$

$c = Specific\ Heat\ (J/Kg \cdot\ K)\ 712\ for\ Si$

$h = Heat\ Transfer\ Coefficent\ (W/m^2\ \cdot K)$

$A_S = Surface\ Area\ (m^2)$

$\theta_i = T_i - T_\infty$

$\theta = T - T_\infty$

And

$T = Temperature\ Setpoint\ (K)$

$T_i = Object\ Initial\ temperaure\ (K)$

$T_\infty = Air\ temperature\ (K)$

It should be noted that the object initial temperature T_i and the air temperature $T\infty$ will be at the same temperature, this means that Θ_i would be zero and so Equation 2-4 above can be reduced to Equation 2-5 for rising transient temperature.

$$t = \frac{\rho V c}{h A_S} \ln \theta \qquad \textbf{Equation 2-5}$$

The heat transfer coefficient h is for the boundary between the solid and the air, typical values for free convection of air would be 2 to 25 (W/m^2 . K), 2 being a low flow of air, 25 being higher, 2 is used in Figure 2-7 and Figure 2-8 below, due to this being the worst case as the cooling effect is less with a low flow of air.

Figure 2-7 below shows the results of Equation 2-5 above for an increase in temperature of 50 °C, and Figure 2-8 below shows the results of Equation 2-5 above for a decrease in temperature of 50 °C, for a solid constructed device and a pillar constructed device. Note the temperature is displayed in °C for convenience it has no effect on the results with this being °C rather than Kelvin (K).

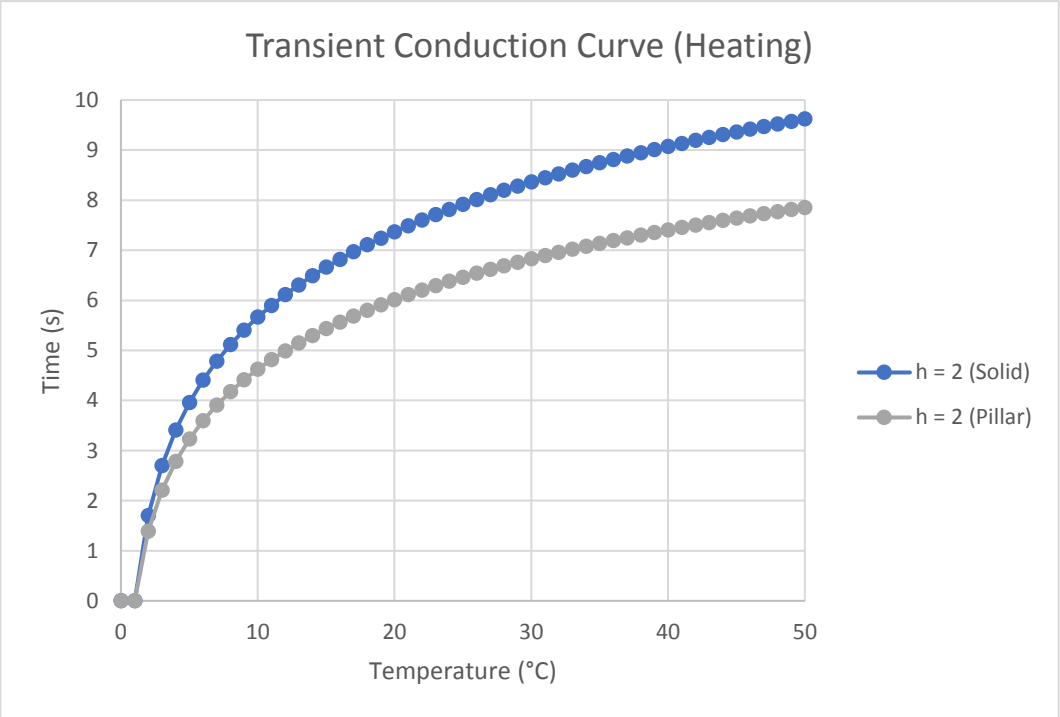

Figure 2-7 - Theoretical transient conduction curve (heating) for solid and pillar diodes

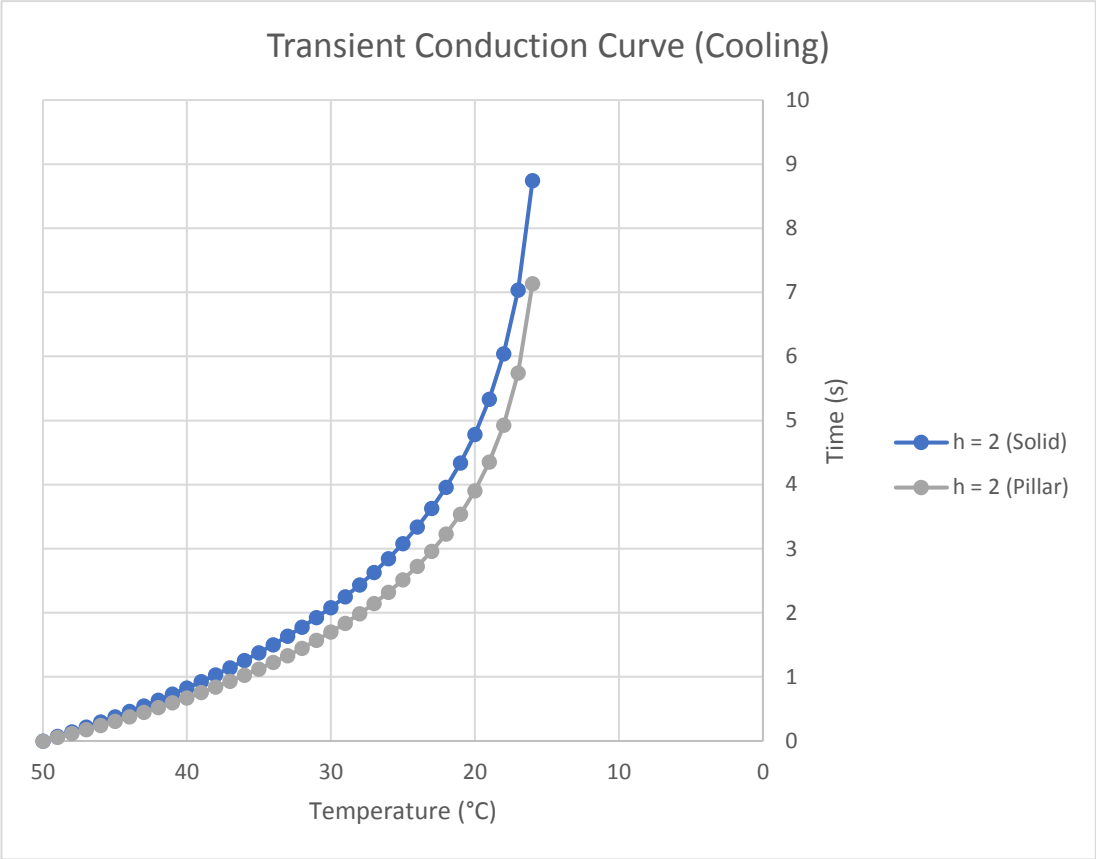

Figure 2-8 - Theoretical transient temperature curve (cooling) for solid and pillar diodes

Figure 2-7 above shows that the devices made from pillars have a higher rate of increase in temperature, when compared with the solid constructed devices. The pillar devices will take 6 seconds to have a temperature rise of 20 °C, whereas the solid constructed devices will take approximately 7.4 seconds.

Figure 2-8 above shows that the devices made from pillars have a higher rate of decrease in temperature, when compared with the solid constructed devices. The pillar devices will take 4 seconds to reach a temperature of 20 °C, whereas the solid constructed devices will take approximately 4.8 seconds.

2.7.3 **Convection**

Convection is the transfer of heat from an object, to the fluid (or gas / air) passing over the object, when there is a temperature difference between the two. In this

research the fluid will be the air around the devices, and the transfer will be by natural convection as opposed to forced convection with a fan. The devices will be hotter than the air, and so the heat will be transferred from the diode to the air, the fact that heat in the air will rise will generate a natural buoyancy driven convection.

Calculations with regard to convection by themselves will not be carried out, so the results will be restricted to the surface temperature of the diodes, where the air around the devices is taken into account, with the lumped capacitance method used for transient conduction.

2.7.4 **Radiation**

This method of heat transfer is by electromagnetic waves emitted from the object, which is due to the heat of the object, mainly in the infrared range, from the surface of the object to the atmosphere around the object, as a consequence of thermal agitation of its composing molecules [3]. No analysis of this type of radiation will be carried out, as part of this research, due to transient conduction being used by measuring the surface temperature.

2.7.5 **Biot Number**

The Biot number (B_i) named after the French physicist Jean-Baptise Biot, is a dimensionless quantity which is used in heat transfer analysis, to determine the thermal resistance in an object. For values of Biot number which are Bi << 1 (0.1 or lower), the object can be classed as thermally thin and the temperature gradient across the object is negligible. It could be concluded from this, that the smaller the Biot number the lower the internal thermal resistances, and hence the object would transfer heat faster. The Biot Number is defined by the following equation, Equation 2-6.

$$Bi = \frac{hL_C}{k} \qquad \textbf{Equation 2-6}$$

Where;

$h = Heat\ Transfer\ Coefficent\ (W/m^2 \cdot K)$

$k = Thermal\ Conductivity\ (W/m\ \cdot K)$

$Lc = Charcteristic\ Length\ (m) = \frac{V}{A_s}$

And;

$A_S = Surface\ Area$ (m^3)

$V = Volume$ (m^2)

The heat transfer coefficient h is for the boundary between the solid and the air, typical values for free convection of air lies between 2 to 25 (W/m^2 . K), 2 represents a low movement of the air and 25 a higher movement, in this situation 25 is the worst-case scenario as this will give a greater cooling effect, and so this value will be used.

The diodes are made from Si and so k the thermal conductivity of Si is 148 (W/m . K) [15].

The two diode types that are used in this research will be made from a solid pillar, which is 1mm in diameter, and pillars which are 50µm in diameter (400 in total), the 400 50µm pillars will give the same volume as the 1mm diameter solid pillar. Calculating the characteristic length of the two types of diode assuming a height of 3µm gives.

For the 1mm diameter diode;

$$L_c = \frac{\pi\ \times (0.5\ \times 10^{-3})^2 \times 3 \times 10^{-6}}{(\pi\ \times (0.5\ \times 10^{-3})^2) + (\pi \times 1 \times 10^{-3} \times 3 \times 10^{-6})} = 2.964\ \times 10^{-6}\ m$$

For the 50µm pillar diode;

$$L_c = \frac{(\pi\ \times (0.5\ \times 10^{-3})^2 \times 3 \times 10^{-6}) \times 400}{\left((\pi\ \times (0.5\ \times 10^{-3})^2) + (\pi \times 1 \times 10^{-3} \times 3 \times 10^{-6})\right) \times 400} = 2.419\ \times 10^{-6} m$$

The above will give Biot numbers of.

For the 1mm diameter diode;

$$Bi = \frac{25 \times 2.964 \times 10^{-6}}{148} = 5.007\ \times 10^{-7}$$

And for the 50µm pillar diode;

$$Bi = \frac{25 \times 2.419 \times 10^{-6}}{148} = 4.086 \times 10^{-7}$$

As can be seen from the two results above the Biot numbers are much less than 1, and so the internal thermal resistances are negligible, and therefore the simplified lumped capacitance analysis can be used.

For completeness because the etched part is part of a substrate which has been etched away, the Biot number will also be calculated for this separately, this is assuming that the size of the substrate is L=10mm W=5mm H=0.5mm.

The characteristic length will be;

$$L_c = \frac{10 \times 10^{-3} \times 5 \times 10^{-3} \times 0.5 \times 10^{-3}}{(5 \times 10^{-3} \times 10 \times 10^{-3} \times 2) + (5 \times 10^{-3} \times 0.5 \times 10^{-3} \times 2) + (10 \times 10^{-3} \times 0.5 \times 10^{-3} \times 2)}$$
$$= 2.1739 \times 10^{-4}$$

This will give a Biot number of;

$$Bi = \frac{25 \times 2.1739 \times 10^{-4}}{148} = 3.6722 \times 10^{-5}$$

Again, this is much less than 1 and so can be treated as thermally thin with no temperature gradient across it. Due to the substrate part being common to both types of diodes, this will not be included in any further analysis.

2.7.6 **Surface temperature**

For a device to be operating at a lower temperature, it could be assumed that if the temperature gradient across the device is negligible, then the temperature of the device will be the surface temperature. Incropera et al [3] states that the surface temperature of a radial system can be calculated from;

$$T_s = T_\infty + \frac{\dot{q}\, r_o}{2h} \qquad \textbf{Equation 2-7}$$

Where;

$T_s = Surface\ temperaure\ (K)$

$T_\infty = Air\ Temperaure\ (K)$

$$\dot{q}(Solid) = \frac{I * V}{Volume} = Rate\ of\ Energy\ Generation\ per\ Unit\ Volume\ \left(\frac{W}{m^3}\right)$$

$$\dot{q}(Pillar) = \frac{I * V * No.of\ Pillars}{Volume}$$

$$= Rate\ of\ Energy\ Generation\ per\ Unit\ Volume\ \left(\frac{W}{m^3}\right)$$

$r_O = Radius\ (m)$

$h = Heat\ Transfer\ Coefficent\ (W/m^2\ \cdot K)$

And Where;

$I = Current\ (A)$

$V = Voltage\ (V)$

$Volume = volume\ of\ the\ strcture\ (m^3)$

Substituting the values into Equation 2-7 above, gives the graph as shown in Figure 2-9 below, for the solid constructed diodes and the pillar constructed diodes. It can clearly be seen that the diodes constructed from pillars have a lower surface temperature, than those constructed from a solid, due to the combined heating and cooling of devices having a larger surface area to volume ratio, as discussed by Palninsic et al [7].

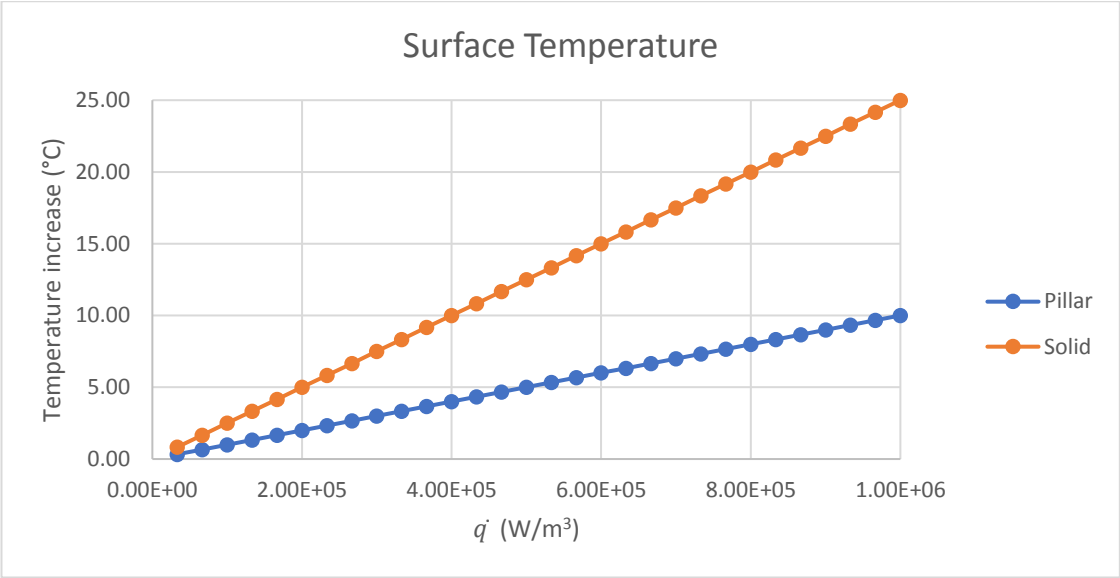

Figure 2-9 - Theoretical surface temperature graph of pillar and solid constructed diodes

2.7.7 Heat transfer summary

The above sections have identified that the devices constructed from pillars, will have the following characteristics compared to the solid constructed devices.

- A lower Biot number
- A faster transient conduction
- A lower surface temperature

Due to the nature of the construction of the diodes in this research, where they share a common substrate, running a long temperature test, and seeing what the final surface temperature of the diode would be is impractical. This is due to the temperature of the substrate overwhelming the temperature of the diodes, due to its large volume compared to the diodes. For this reason, this research will be looking at the transient conduction, and a faster temperature increase and decrease for the pillar diodes compared to the solid diodes. This test is run for a short period of 10 seconds, therefore, during this short period the substrate will have less effect on the readings obtained.

2.8 Literature Review Summary

The review of the literature has provided an insight into the research that has been carried out on nanowires, for use in a power Schottky diode, and the implications of elevated temperatures on the diodes, with the increase in forward

and reverse biased currents, as the temperature of the diode increases. At present there is little literature on the temperature measurements of diodes made from a pillar construction, and the enhanced heat dissipation which can be achieved from this type of diode with an increase in the surface area to volume ratio.

Chapter 3 **Electrical Characteristic Techniques**

3.1 **Introduction**

Characteristic measurements are used to determine how good devices are performing, with regard Schottky diodes the important characteristics are:

- Forward bias turn on voltage
- Reverse bias leakage current
- Ideality factor

3.2 **Forward Bias turn on voltage**

When a metal comes into intimate contact with a semiconductor a barrier is formed, the height of this barrier is determined by the work functions of the metal and the semiconductor [15]. The barrier needs to be overcome for conduction to take place, the higher the barrier the more potential across the barrier is required to overcome it. The height of this barrier will determine the forward biased turn on voltage of the Schottky diode.

The typical forward biased turn on voltage for a Si Schottky diode would be in the region of 0.15 Vdc to 0.45 Vdc, manufactures of diodes call this the forward voltage drop V_F and provide graphs on their data sheets of forward voltage verses forward current. ON Semiconductor data sheet [74] for an 1N5817 Schottky diode shows this as 0.22 Vdc @ 20mA, Fairchild data sheet [75] for an SB120 Schottky Diode shows this at 0.36 Vdc at 100mA, Radio Spares data sheet [76] for an MBR1100 Schottky Diode shows this as 0.41 Vdc at 20mA, and Mohan et al [14] states this as 0.3 Vdc to 0.4 Vdc. The forward bias turn on voltage is determined by plotting an I-V curve for the diode. As an example,

Figure 3-1 below shows an I-V curve for a diode made at DMU and a production diode type 1N5817.

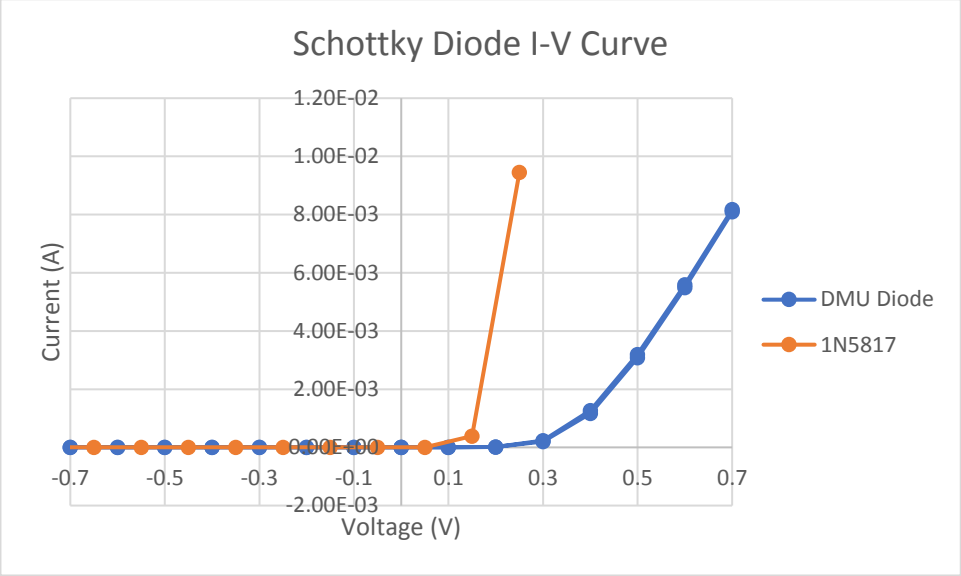

Figure 3-1 - DMU and 1N5817 Schottky diode I-V curves

It can be seen from

Figure 3-1 that the turn-on voltage is in the region of 0.3 Vdc for the DMU diode and 0.1 Vdc for the 1N5817, with steps in voltage of 0.1 Vdc, which are both in the expected range.

The I-V measurements are carried out by applying a stepped voltage across the diodes and measuring the corresponding current, a HP4140B that is connected to a PC via GPIB is used for this, the PC is running a program on Agilent VEE which performs the stepped voltage, and collects the data and outputs this to a .csv text file. A photo of the HP4140B is shown below in Figure 3-2 and Figure 3-3 below shows how the equipment is connected together.

Figure 3-2 - HP4140B Meter / DC voltage source photo

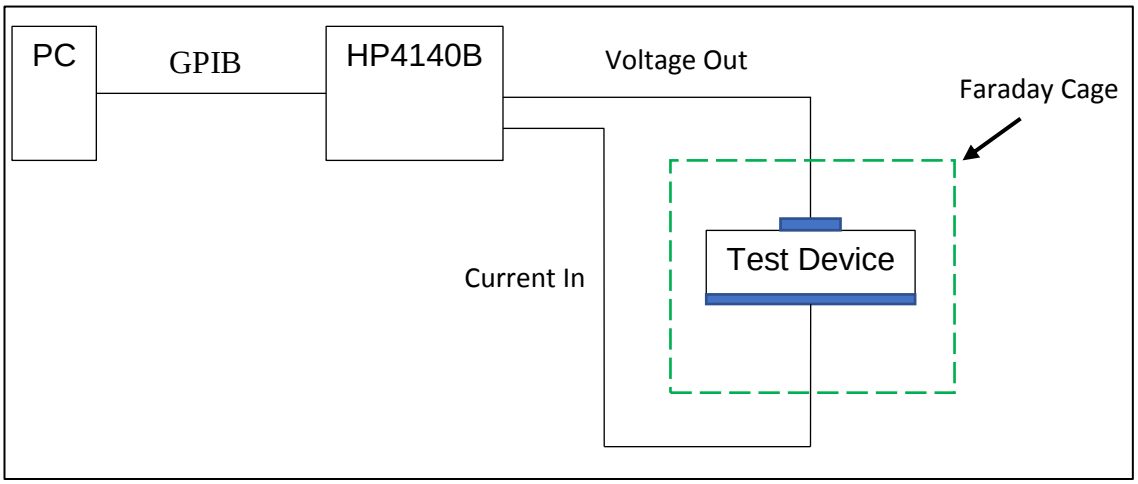

Figure 3-3 - I-V Test equipment connection diagram

Due to the samples not being completely covered, light will have an impact on the readings obtained, therefore all readings will be taken with the samples in a Faraday cage as indicated by the dotted green line in Figure 3-3 above.

3.3 Reverse Bias Leakage current

The amount of reverse leakage current is determined by the barrier height and the reversed biased potential, the lower the barrier height the easier it is for the minority carriers to overcome the barrier. With an increase in reverse potential the minority carriers have more energy and can overcome the barrier easier, with an increase in reverse leakage current. When selecting the contact metals there will always be a compromise between the turn on voltage and reverse leakage current.

The reverse bias leakage current needs to be as low as possible, Mohan et al [14] states that the reverse leakage current of a Schottky diode is higher than that of a P-N junction diode, but gives no values, from the manufactures diode data sheets [74][75][76], the range of reverse current at the rated reverse voltage is in the range of 0.5mA to 1mA, typically in the micro Amps range.

It is usual to compare the ratio of the forward biased current to the reverse biased leakage current, the rectification ratio. A ratio of above two orders is thought to be good, but is subjective and dependant on the voltages at which the current is taken. This is good for comparison purposes with similar diodes, the higher the rectification ratio the better the diode. Figure 3-4 below shows the graph used for comparison, of the DMU diode and a production 1N5817 diode, the log of the current is plotted.

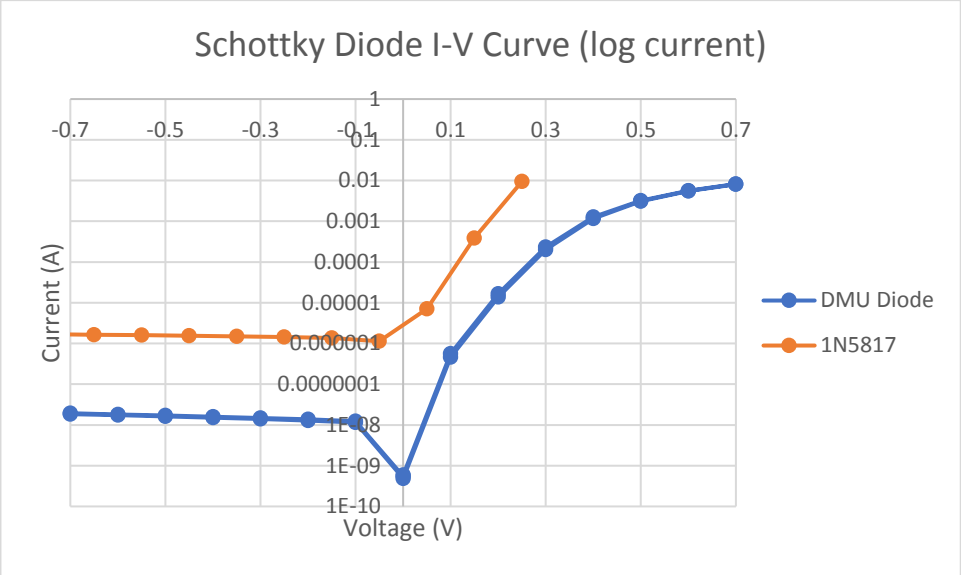

Figure 3-4 - DMU and 1N5817 diode reverse leakage current I-V graph

The rectification ratio is calculated from Equation 3-1 below.

$$RR = \log\left(\frac{I_{forward}}{abs\ I_{reverse}}\right) \quad \textbf{Equation 3-1}$$

Where;

RR = rectification ratio

$I_{forward}$ = Current at the forward biased voltage (A)

$I_{reverse}$ = Current at the reversed biased voltage (A)

The forward and reversed biased voltage should be of the same magnitude but opposite signs. For a forward biased voltage of +0.7 V and reversed biased voltage of -0.7 V, the rectification ratio for the DMU diode depicted in Figure 3-4 above is shown in Table 3-1 below.

DMU Diode - Rectification Ratio			
Diode No.	Pillar Diode		
	Current (A) @		Ratio
	-0.7v	+0.7v	
	-1.85E-08	8.10E-03	5.64

Table 3-1 - DMU diode rectification ratio calculation

The readings used for this characterisation are the same as the ones taken for the forward biased turn on voltage above, just displayed in a different manner.

3.4 Ideality Factor

This is a measure of the quality of the diode, a factor of 1 [9] would indicate an ideal diode, the closer the value is to one the better the quality of diode.

The equation for determining the ideality factor [15] is shown in Equation 3-2 below.

$$\eta \equiv \frac{q}{kT}\frac{dV}{d(lnJ)}$$

Equation 3-2 - Ideality Factor

Where;

q is the electronic charge (C) (1.69E-19)

k is Boltzmann's constant (J/K) (1.38E-23)

T is the temperature (K) (300)

V is the voltage across the diode (V)

J is the forward biased current (A)

The ideality factor is obtained from the I-V curve and Equation 3-2 above, which is basically a change in forward biased voltage and the corresponding change in natural log of the current.

For the I-V curve shown in

Figure 3-1 above the ideality factor of the DMU diode for a temperature of 300 K, with the change in voltage being 0.7Vdc – 0.6 Vdc = 0.1 Vdc, and the current readings being for 0.7 Vdc is $8.18E^{-3}$ A and for 0.6 Vdc being $5.59E^{-3}$ A, the Ideality factor calculation is shown in Table 3-2 below.

DMU Diode				
Pillar Diode				
V1	V2	J1	J2	**η**
0.60	0.70	5.59E-03	8.18E-03	**10.15**

Table 3-2 - DMU diode Ideality factor calculation

As discussed in chapter 2, the ideality factor can have a wide range, the above is high but is within the expected range.

Chapter 4 **Physical Characteristic Techniques**

These measurement techniques have been utilised to check the manufacturing process.

- Optical Characterisation
- Surface analysis
- Profile thickness measurement

4.1 **Optical Characterisation**

Optical measurements are usually non-contacting with minimal sample preparation required, and very versatile. There are four main optical techniques where the light is either reflected, emitted, transmitted or absorbed, these are described by Schroder [77] and shown in Figure 4-1 below, *hv* being the energy.

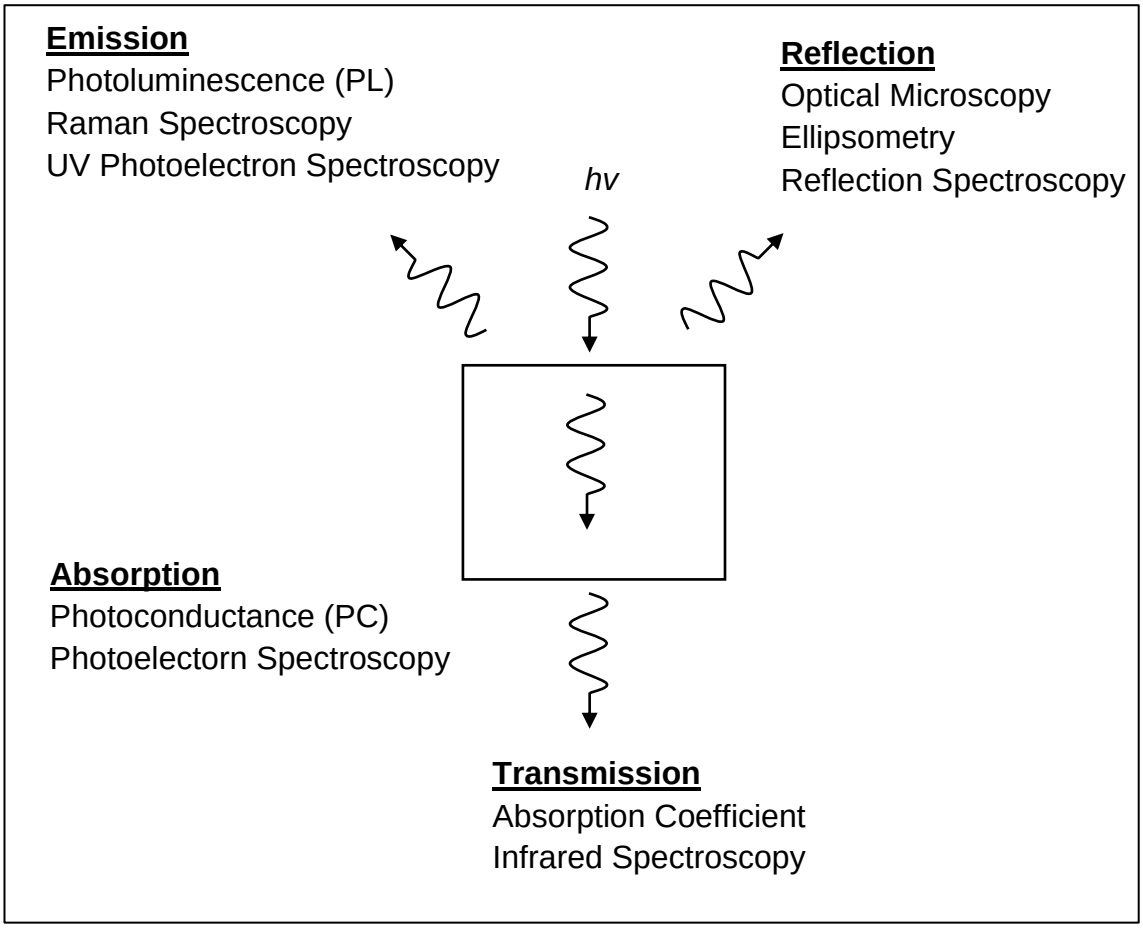

Figure 4-1 - Optical characterisation techniques diagram

In this research the reflection technique has been used in the form of;

- Optical Microscopy (Optical Microscope)
- Ellipsometry

Optical characterisation is a visual technique which allows the features of an object to be investigated. It is usual that some form of magnification is required, optical microscopes are useful for sizes above 0.5µm, for smaller sizes electron beam microscopes (SEM) are used [77].

4.1.1 **Optical Microscope**

An optical microscope is a relatively simple device using lenses, the eye piece and the objective, to view a real enlarged image. Some form of illumination is also required, this can either be from above or below, usually above for non-transparent materials.

The optical microscope which has been used is a Nikon labophot 2 upright type, as shown in Figure 4-2 below, this has various magnifications of 4x, 10x, 40x and 100x.

Figure 4-2 - Nikon Labophot 2 microscope optical microscope photo

The optical microscope has been used to look at the quality of how the photoresist has been applied to the samples, and the definition achieved, including measurements of the size of the photoresist on the samples. Also, images of the

etched samples shall be obtained to determine how good the etching process has been. An example of the imagery obtained of the photoresist is shown in Figure 4-3 below.

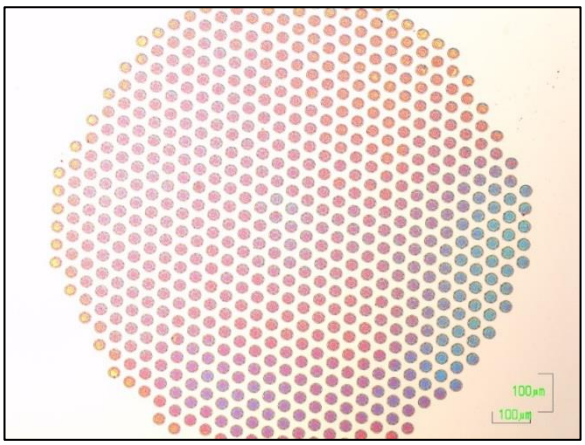

Figure 4-3 - Optical microscope photoresist image

4.1.2 **Ellipsometer**

Ellipsometer measurements have been used to determine the thickness of SiNx that has been deposited on the samples, and for this a Rudolph Auto EL Ellipsometer has been used. This uses a polarised reflected light, off the surface of the sample, to determine the thickness of films. This is a very accurate method of measurement, and can measure from a few Angstroms to tens of microns in thickness. Figure 4-4 below gives an illustration of the Ellipsometer. The infrared source is a laser, this passes through a polariser which alters the light wave in the S and P planes, such that an ellipical pattern can be achieved, hence the name of the device. This is then reflected off the surface of the sample, where some of the light will be absorbed and some reflected, the reflected signal is then passed through the analyser and then onto the detector. The device compares the orignal transmitted signal with the received one and gives values of thickness and refractive index (IR).

For SiNx Mih [78] suggests that the IR should be in the range of 1.83 - 2.03 for a ratio of 0.1 to 0.5 of NH_3 / SiH_4.

A ratio of 10/90 for NH_3 / SiH_4 will be used, which is 0.111, therefore the expected IR would be just above 1.83, the average IR that was measured from a number

of measurements is 1.85, thus there is a high confidence that the measured thickness is that of SiNx.

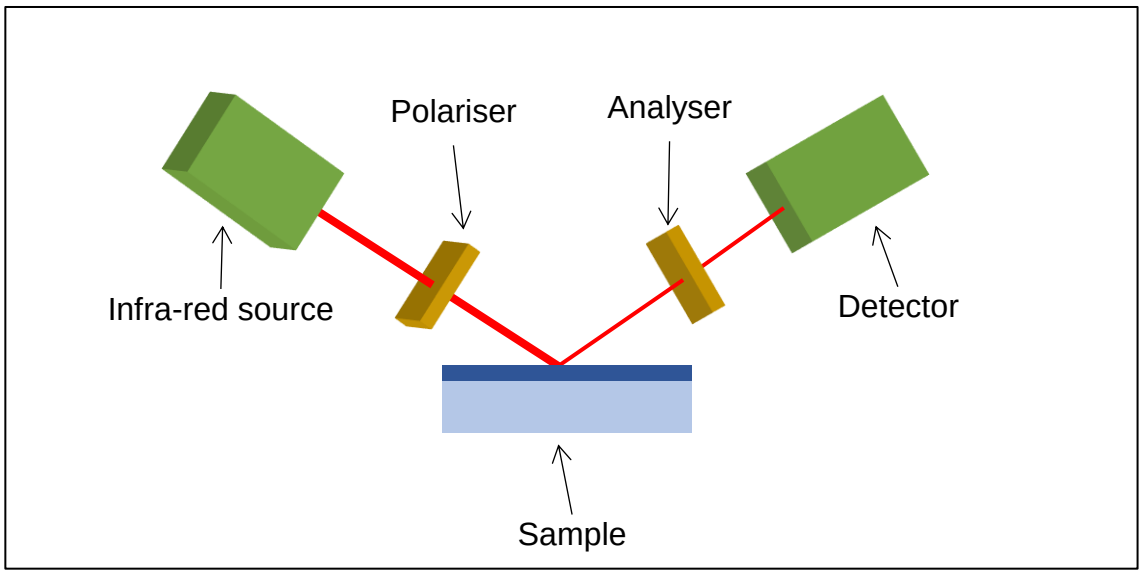

Figure 4-4 - Ellipsometer diagram

Figure 4-5 below shows a picture of the actual Ellipsometer used.

Figure 4-5 - Photo of Ellipsometer equipment

4.2 Surface Analysis - Scanning Electron Microscope

The Scanning Electron Microscope (SEM) is a device which allows high magnification to be achieved, allowing objects to be examined in detail, as well as top down images, it is possible in an SEM to tilt the objects to gain information with regard height, and to give a 3D type of image. The samples are placed onto

the chuck inside the chamber, and then evacuated of air with nitrogen, and pumped down to approximately 100mbarA. Highly concentrated electrons are generated and focused onto the sample, and when these interact with the sample, low energy secondary electrons and high energy backscattered electrons are produced. These signals are collected by detectors and used to build up an image of the surface [79]. The area of the sample is scanned sequentially to build up the picture, various magnifications are available by adjusting the electron energy and the size of the focused beam. In addition, the SEM can also provide measurements and the images can be saved.

The SEM that has been used is a LEICA S430 as shown in Figure 4-6 below, this will be used for looking at the final etched samples. An example of the type of imagery obtained is shown in Figure 4-7 below, this is the image of photoresist on one of the samples.

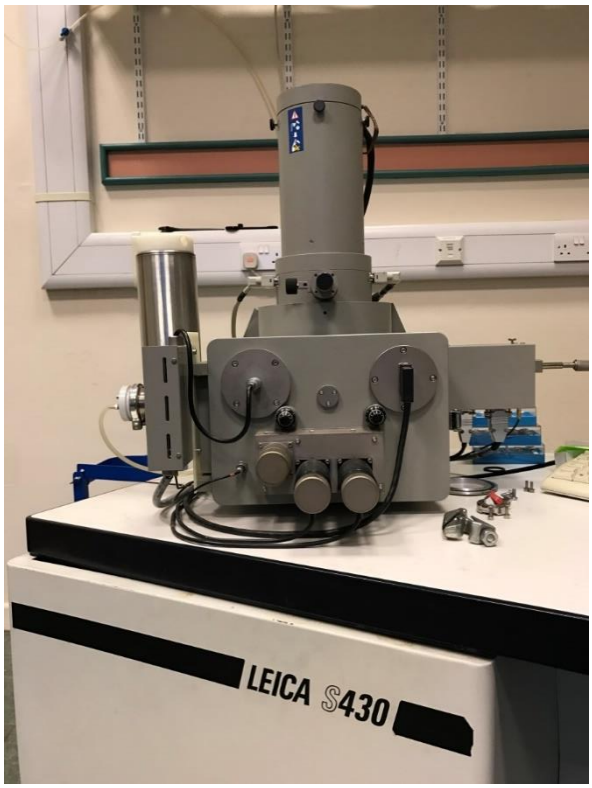

Figure 4-6 - Leica S430 SEM equipment photo

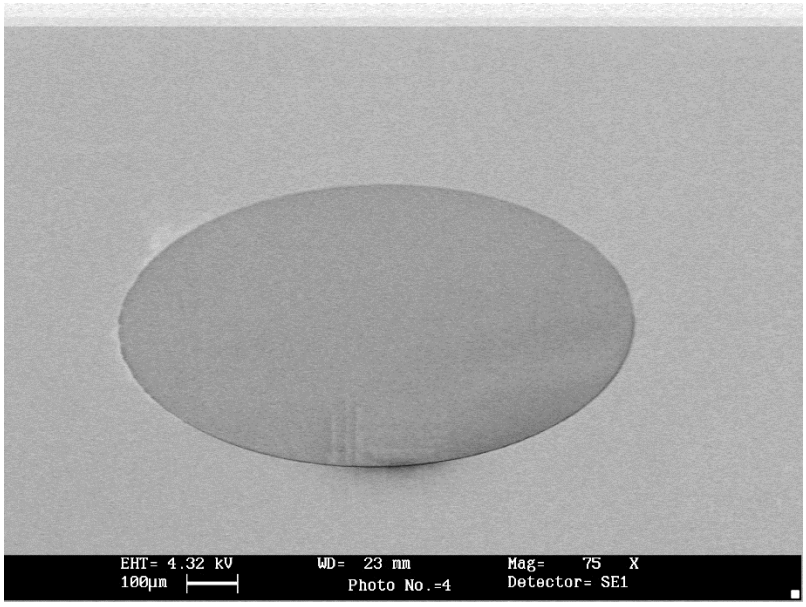

Figure 4-7 - SEM Image of photoresist

4.3 **Profile Thickness Measurement**

Profile measurement allows the surface of an object to be measured, this can be for surface roughness or features which have been created, there are two main types that are used these are;

- Mechanical Profilometers
- Optical Profilometers

The stylus types apply a very small force in contact with the surface, then stepped across the surface and a deflection in the height of the stylus is recorded, this can leave small marks on the surface of soft materials.

The optical type usually uses a laser, which is projected onto the surface and reflected. The time delay in the reflected light is recorded and this is correlated to the height measurement. It should be noted that objects which are transparent to the laser light will not be able to be measured with an optical profilometer.

A stylus type profilometer will be used, this shall be a Tencor alpha-step 200 device as shown in Figure 4-8 below.

Figure 4-8 - Profilometer equipment photo

The Tencor can be setup to allow different lengths to be scanned and at two different resolutions, the plots shall mainly be using 2000µm (2mm) length and at a resolution of 1 step per µm, which will give 2000 readings. The Tencor also allows the data to be levelled if required. The stylus fitted has a radius of 12.5µm, this means that the full depth of channels smaller than 25um cannot be measured. The stylus tracking force used was set to 8mg.

The data from the profilometer is printed to a PC via the RS-232 printer port, this data is then captured by an RS-232 serial port monitor and stored into a text file. The text file is then loaded into Excel, and the data is then sorted to enable a graph to be produced. Figure 4-9 below shows a typical graph which is obtained from the profilometer for a pillar type diode.

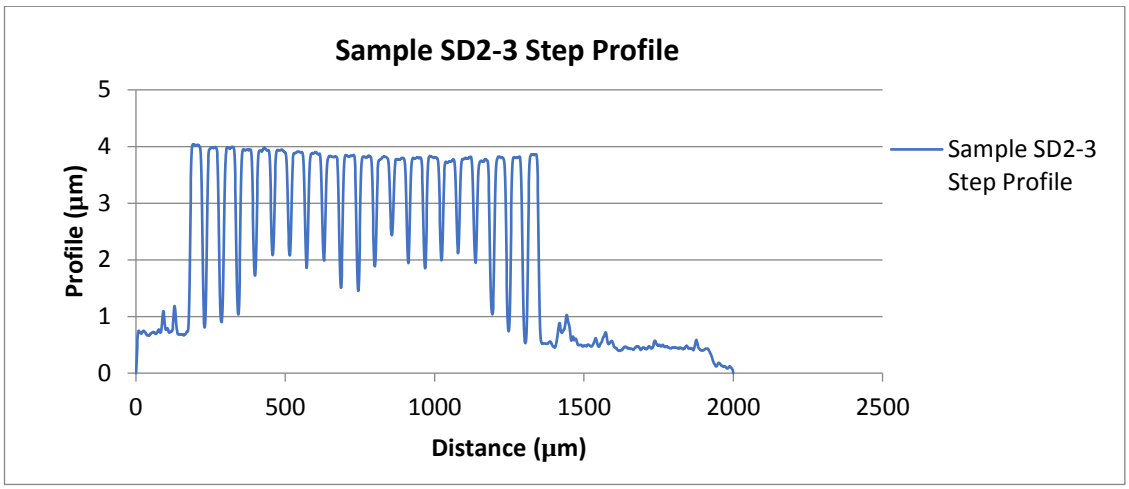

Figure 4-9 - Tencor step profile plot of a pillar diode

Chapter 5 **Design and implementation of electrical measurement for heat loss**

5.1 Introduction

The first three Schottky diode electrical characteristics, as discussed in Chapter 3, are used to determine how good the device is against an ideal Schottky diode. The forward bias turn voltage for Si should be between 0.15V and 0.45V, and the reverse bias leakage current should be as low as possible, typically in the μA range and the ideality factor should be as close to 1 as possible.

The device temperature is used to ensure that the maximum operating temperature of the device is not reached, for Si this is around 100 - 200 °C [14], where the device will break down beyond recovery. In addition, as discussed in Chapter 2, as the temperature of the diode increases so does the forward and reverse biased currents. This rise in current reduces the energy efficiency of the diodes.

This chapter demonstrates a practical method of measuring the temperature of a Schottky diode, constructed as part of this research, and to ascertain the transient temperature rise and fall of the surface temperature, for comparison of the two different types of diodes.

5.2 Temperature Measurement

Due to the method of manufacture of the diodes on different sized substrates, it is difficult to obtain a comparison of the operating steady state temperature of the diodes, due to the substrate having an effect on the temperature. Instead, it is proposed to measure the rising and falling temperature rates for a fixed current, as discussed in chapter 2, where the diodes made from pillar construction will have a faster rising and falling temperature. These tests run over a short period of time (10 seconds) should eliminate, to a certain extent, the effect of the substrate on the temperature measurements, and allow a comparison to be made.

There was no test set up at DMU for the measuring of device temperature, and so one had to be devised to carry this out. Thermocouples have been used because of their large temperature ranges, but the accuracy and repeatability of the devices is not as good as a Resistance Temperature Device (RTD). The accuracy of the temperature device is not important to the tests, but the repeatability is, and as such an RTD shall be used for the temperature measurements.

The RTD temperature probe used is a class ‘A’ accuracy (+/- (0.15 + 0.002* t, t being the temperature of interest) thin film PT100, this has a very small surface area and responds very well to changes in temperature. This is placed on to the top Al contact and held in place with a small force from above. The PT100 is a device whose resistance changes with temperature, the device has a resistance of 100 ohms at 0 °C and has a α of 0.385 ohms per °C, the Keithley 195A will be used to convert this resistance to °C.

In addition to the Keithley 195A, the test equipment set-up for the measurement of temperature will consist of the following equipment.

- PC
- Keithley 195A (Temperature measurement)
- Keithley 220 (Constant Current Source)
- HP3438A (Voltage Measurement)

These will all be connected as shown in Figure 5-1 below, and a photo of the equipment used is shown in Figure 5-2 below.

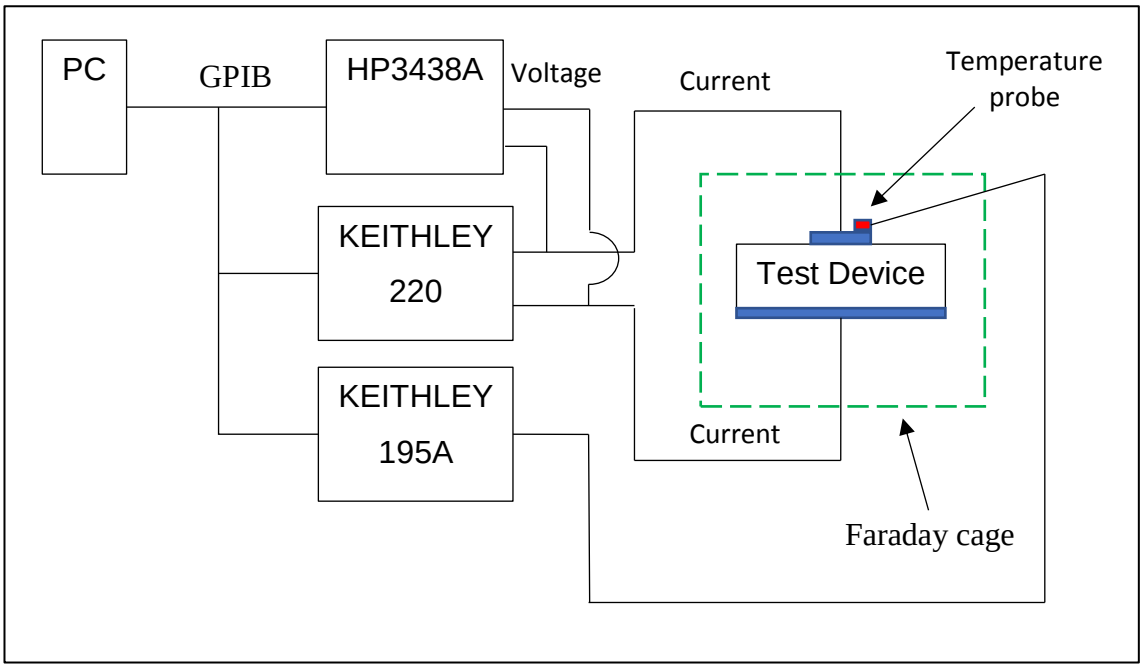

Figure 5-1 - Temperature measurement equipment connections diagram

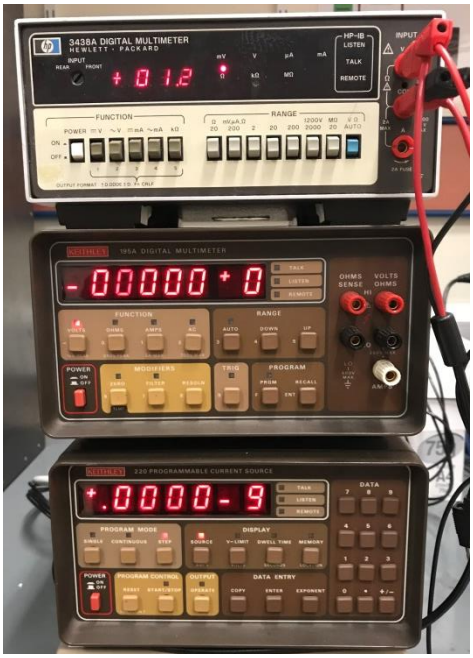

Figure 5-2 - Temperature measurement equipment photo

Figure 5-3 below shows an actual test setup with the sample, test probes and RTD.

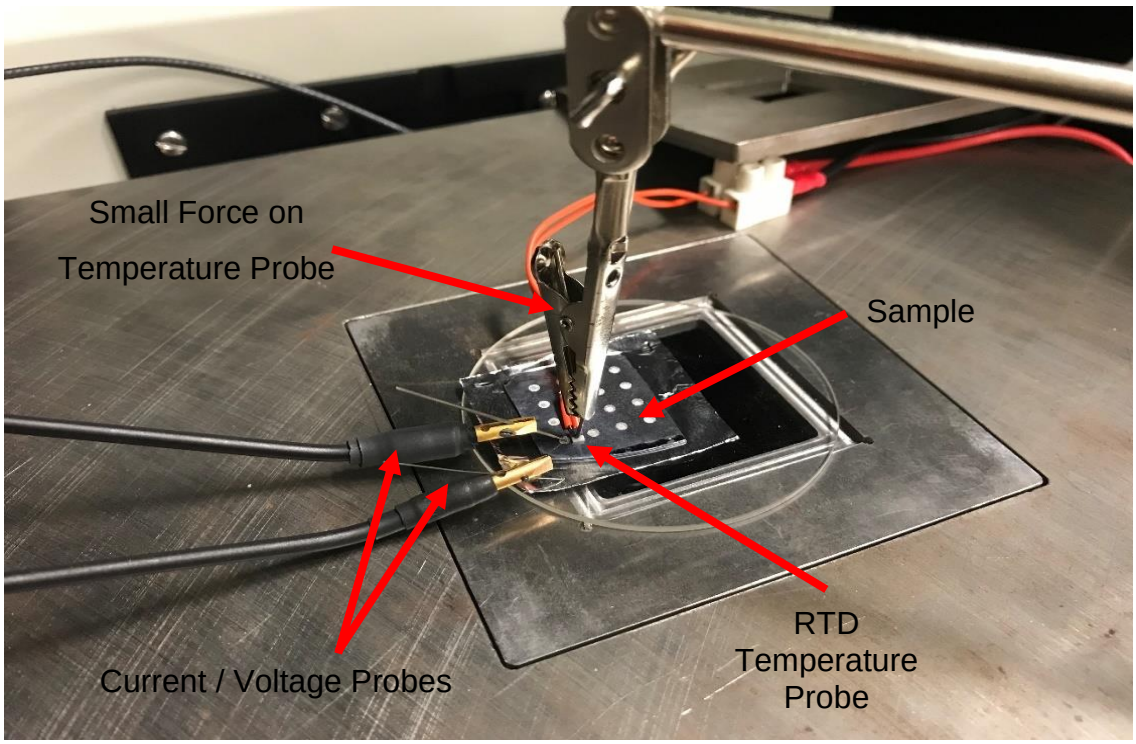

Figure 5-3 - Temperature measurement test setup photo

The measurement devices as detailed above are programed and controlled over the GPIB connections, which are connected to a PC running the Windows© operating system and the Agilent VEE© programme. A new program to apply the current and measure the voltage and temperature has been created.

The temperature program applies a defined current which is set by the user, the values used have been 50mA and 100mA. These values are arbitrary, 100mA is the maximum output from the current source, but these were found to give a good change in temperature. The current is held for a period of approximately 10 seconds, after this period the current is removed and held for a further 10 seconds. The program allows for a number of cycles to be carried out which are set by the user. Five cycles have been used, and the user can set a dwell time between cycles, here 60 seconds has been used, this was found to be an appropriate time so that the temperature of the diode returned to ambient.

Current, voltage and temperature readings are taken, and time stamped every second except during the dwell time for the complete test run time, this gives a total test run period of approximately 5 minutes 30 seconds.

With having a test period of approximately 5 minutes, it is considered that any changes of ambient temperature would be minimal, if any, and so this would not affect the results obtained and have not been recorded.

Typically, two different currents are applied in the forward bias region of the Schottky diodes, to provide two sets of temperature rising and falling readings. From earlier tests carried out, where three sets of readings were taken, it was found that the average power vs average temperature difference was a linear relationship, and hence there was no need to carry out three sets of readings. Figure 5-4 below shows a temperature test carried out which used three currents of 50mA, 75mA and 100mA, as can be seen this is a linear relationship, and hence no need to carry out more than two readings.

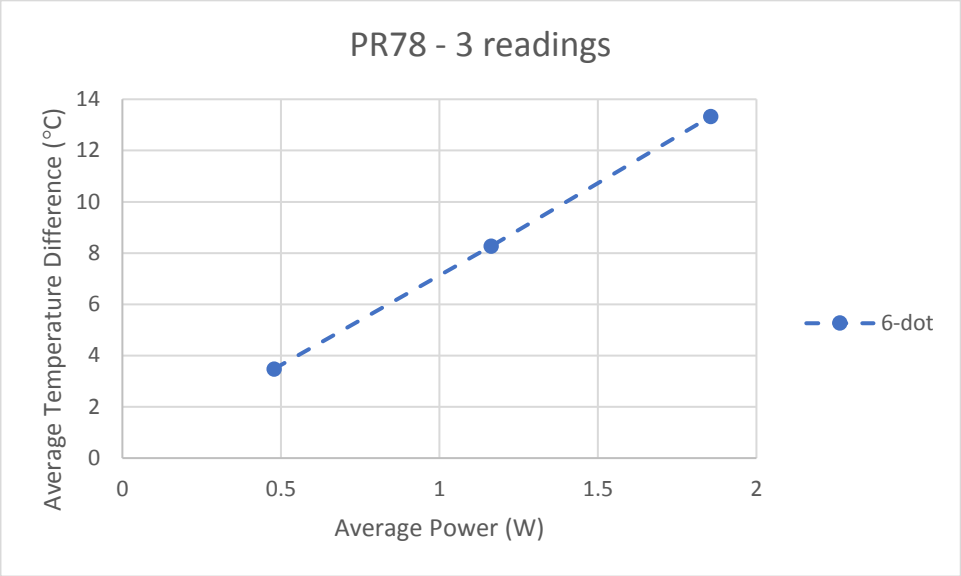

Figure 5-4 - PR78 Three readings of average temperature difference vs average power

The voltage and current readings obtained were used to provide the power dissipated. Figure 5-5 below is a screen shot of the program after a temperature run.

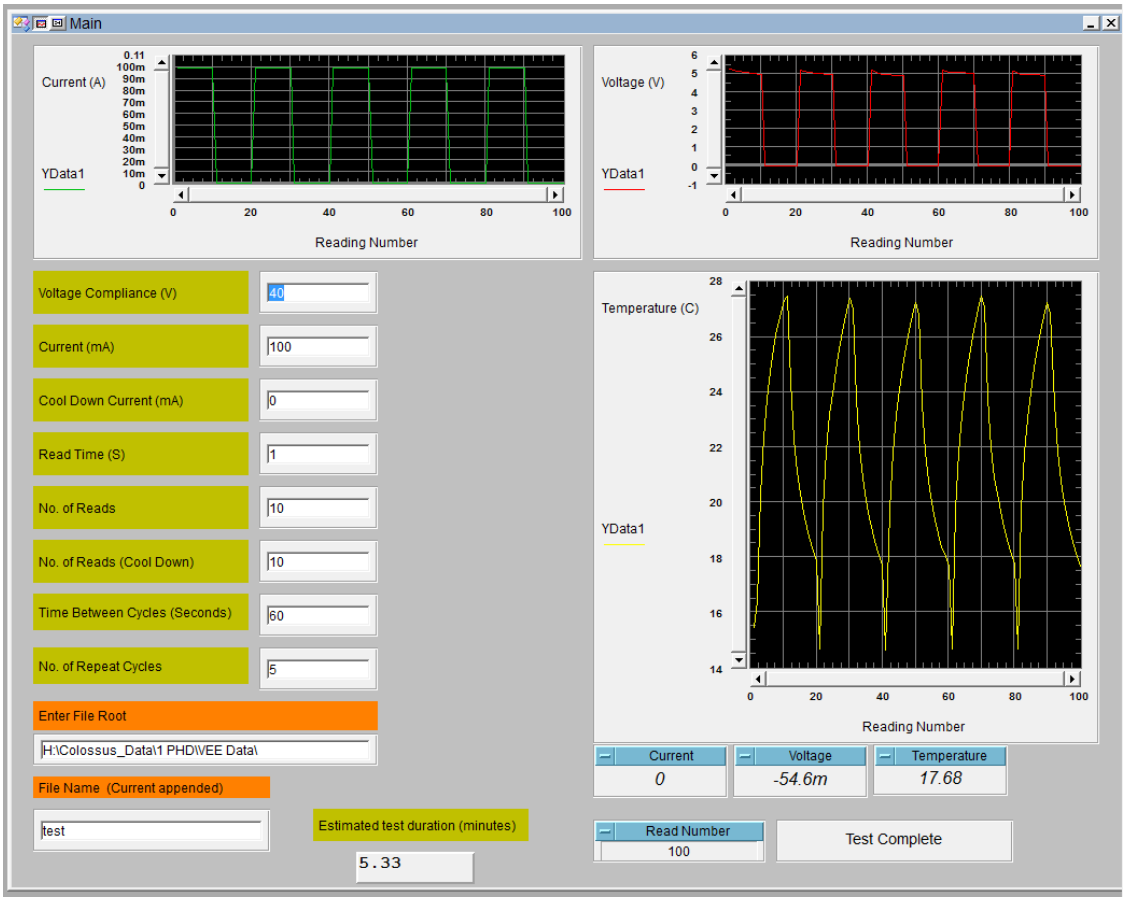

Figure 5-5 - VEE Temperature program screen shot

The data from the tests is automatically stored into a text delimited file, which is imported into Excel for further examination. Figure 5-6 below shows the temperature, Current and Voltage readings obtained for SD2-6, the blue line being the temperature which shows an increase when the current is applied, and then falling away when the current has been removed. The red line shows the voltage as a consequence of 100mA being applied to the diode, this also shows that while the current is applied the voltage decays slightly, this would correspond well with the fact that as the diodes temperature increases the current will also increase, as discussed in chapter 2, and to maintain a constant current of 100 mA the voltage must reduce. The green line shows the current.

From the five cycles which are taken, the first cycle is ignored, the further four cycles are averaged out to give, average voltage, the average of when the current is applied as shown at area A on Figure 5-6, and average temperature change, rising, between points X and Y on Figure 5-6, and falling between points Y and Z on Figure 5-6 (the current is constant).

The average voltage and current are multiplied together to give the average power, the amount of power being dissipated does have an effect on the temperature rise and fall measurements, the more power the higher temperatures achieved.

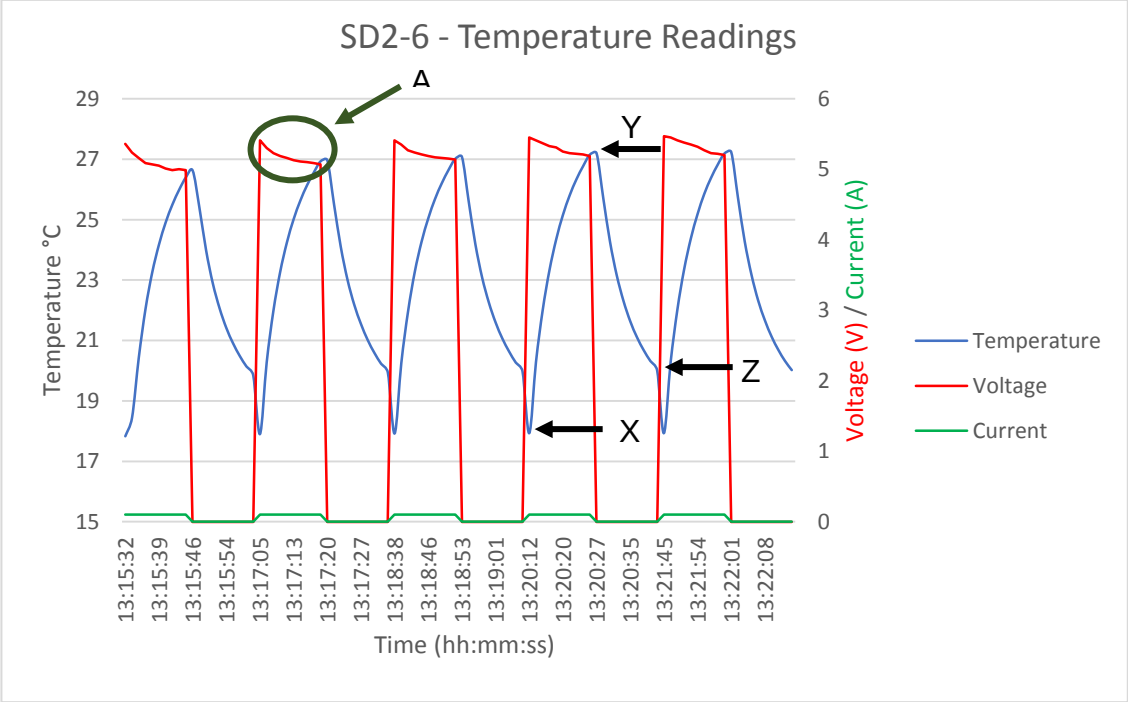

Figure 5-6 - SD2-6 Temperature readings with current and voltage showing (A) Voltage (X-Y) temperature rise and (Y-Z) temperature fall

The average power and average temperature difference (rising and falling) are then plotted for the two different currents, See Figure 5-7 and Figure 5-8 below.

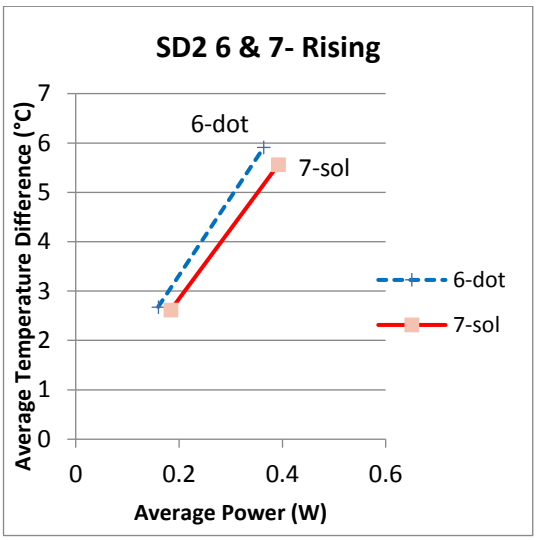

Figure 5-7 - Pillar and solid diode temperature rising graph

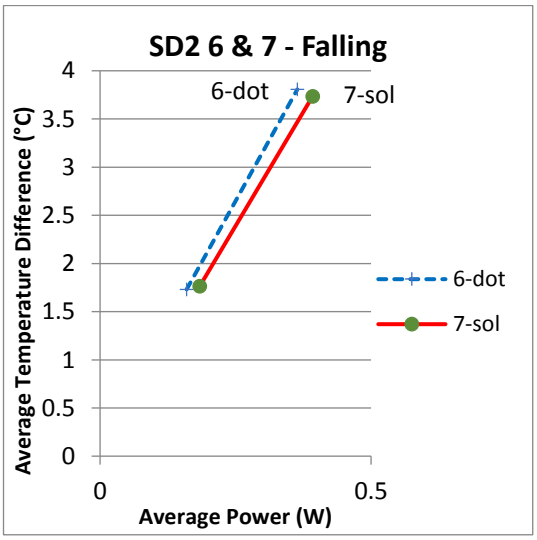

Figure 5-8 - Pillar and solid diode temperature falling graph

The 6-dot represents the pillar constructed diodes, and the 7-sol represent the solid constructed diodes. As can be seen from the above two plots, the pillar constructed devices have a faster temperature rise and fall, than those made from the solid construction, and hence will have a lower operating temperature, as discussed in chapter 2.

Chapter 6 **Optimisation of the PECVD process for making pillars (CF_4 Etching)**

This section of the thesis describes the work that has been carried out on the optimisation of CF_4 etching of Si as part of this research.

6.1 **Overview**

Plasma etching of Si in fluorocarbon gases is a well proven procedure [68] and has been carried out for a number of years, with gases such as SF_6 and CF_4 with various additives like O_2 to increase the etch rate. However, plasma etching (RIE) of Si with 100% CF_4 is not very much discussed in literature, mainly because of the very slow etch rates which are obtained, however, with a slow etch rate due to lower energy bombardment of CF_4 [68] the damage to the surface is minimised. In addition, CF_4 is usually readily available in an RIE system as this is used as a gas for cleaning the chamber, and is a relatively safe gas to use, and etching can be carried out at room temperature avoiding the need to heat the chamber. This chapter provides literature on published etch rates of Si with CF_4, and details the etch rates obtained when etching Si <100> in 100% CF_4 gas, using RIE with varying flows, pressure and RF power.

6.2 **Introduction**

Dry chemical etching has advantages over wet chemical etching and is the most commonly used method of etching, when small features are required like in VLSI devices [68]. Etching of Si with fluorocarbon gases can be achieved at room temperature, with the ability to control the etch rate and directionality, to produce anisotropy features and cause less damage to the surface. When using CF_4 to etch Si with RIE it is usual to mix this in various ratios with other gases, like Ar [80][81], O_2 [82] and H_2 [83][84], and etch rates have been observed of between 4 nm/min and 178 nm/min. Etching of Si with CF_4 in microwave discharge has been observed at 1300 nm/min [85], which has been stated as an etching rate of one order larger than using RIE, and etching with 100% CF_4 has been observed at approximately 50 nm/min [86][87]. These etch rates are relatively small compared to those that have been observed with wet chemical etching [69], where values of around 1000nm/min can be achieved with KOH. Other issues

with obtaining large etch depths with slow etch rates, is the selectivity of the mask being used, Balachova et al [86] observed that a photoresist gives approximately 1.3:1 to 1.7:1 selectivity, and masks with a high mechanical hardness are required.

Due to the varied range of data available with regard to the etching of Si with 100% CF_4, it was decided that as part of the research, some etching tests were to be carried out, to ascertain the etch depths that could be obtained with the equipment at DMU.

This chapter details experimental results of plasma etching (RIE) of Si with 100% CF_4, the etching has been carried out in a Plasma Technology RIE slave chamber with varying parameters of flow, pressure and RF power.

6.3 Experimental

The samples used for the experiments were Si <100> wafers of random sizes, lightly p-doped, approximately 500µm thick and polished on one side. Al dots of sizes between 0.5mm and 1.5mm diameter were deposited onto the polished side of the wafers, as masks for etching, (Al dots will be etched slightly [69] by the plasma process but not significantly). Figure 6-1 below shows an example of a sample with the Al dots deposited.

Figure 6-1 - Wafer sample with aluminium top Schottky contacts deposited

Once prepared, the samples would be placed onto the lower electrode in the slave chamber, which is capacitively coupled to a 13.56 MHz RF generator, and the chamber left to pump down to a pressure below 30 x 10^{-3} Torr. The CF_4 flow

is adjusted manually with a Rotometer, Figure 6-2 below shows an image of the Rotometer, this has a range of 0 - 9700 sscm with a scale of 0 - 6.5, Table 6-1 below was used to estimate the flow of CF_4 into the chamber.

Figure 6-2 - Rotometer for measuring the CF_4 flow rate

Scale	Actual Flow (sccm)
0	0
0.1	149
0.2	298
0.3	448
0.4	597
0.5	746
1.0	1492
2	2984
3	4477
4	5969
5	7461
6	8954
6.6	9700

Table 6-1 - Rotometer flow rate calibration table scale marking Vs actual flow rate

The pressure within the chamber can be set between 0.060 – 0.25 x 10^{-3} Torr and this is automatically controlled. It should be noted that the system only

allowed the low pressures with a low flow, and still maintain a controlled pressure within the chamber.

The RF power is set between 200 - 250 watts, and the etching durations were carried out for one hour.

6.4 Results and Discussion

Before the etching was carried out, profiles of some of the samples have been taken using an Alpha Step 200 profilometer. The profiles were taken after the Al dots had been deposited onto the samples, Figure 6-3 below shows an example of the profiles taken before etching.

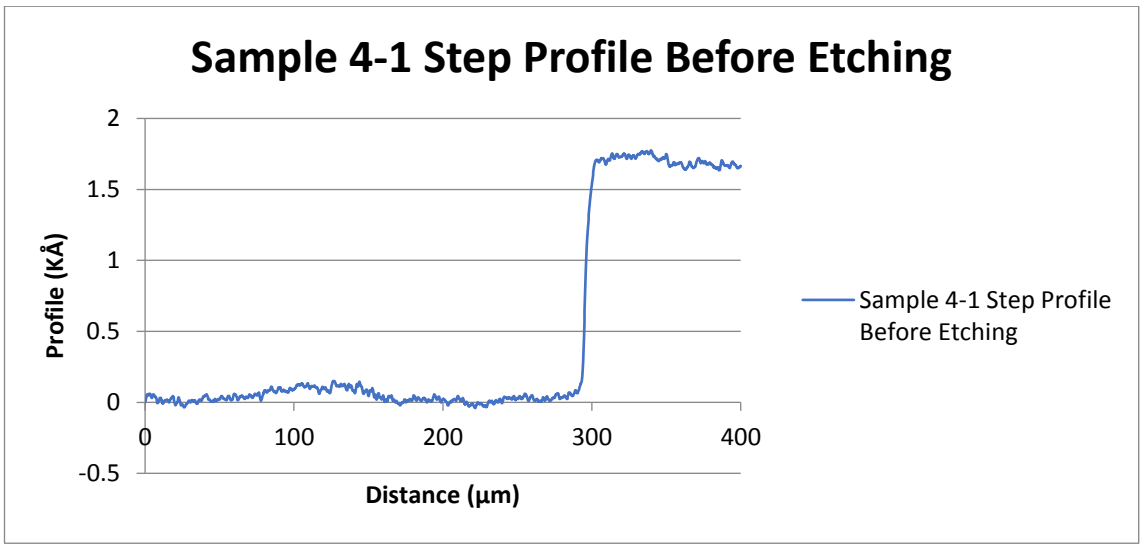

Figure 6-3 - Profile of deposited Al dot before etching showing a thickness of approximately 170nm

The thickness of Al deposited before and after the etching was between 150 – 200 nm.

The profile of the non-etched Si surface has been measured before etching for sample 3, to enable a check to be made after etching, to see if the CF_4 etching causes damage to the surface, 8 sets of readings were taken at different areas on the surface, the average of approximately 500 steps at 0.2µm/step were calculated for each set of readings, by taking the difference from adjacent steps, adding these up and taking the average. The average of these 8 sets of readings was then taken to give an average surface roughness of 0.443nm.

Six tests have been carried out in total with 16 samples being used, the parameters used for the tests are shown in Table 6-2 below.

Test No.	Pressure (x10^{-3} Torr)	Flow Rate (sccm)	Power (w)
1	0.25	1800	200
2	0.2	1800	200
3	0.1	900	200
4	0.06	375	200
5	0.06	375	250
6	0.06	149	250

Table 6-2 - 100% CF4 Si Etching test parameters for pressure, flow rate and RF power

6.5 Test Results

Table 6-3 below shows the results of the etching tests with the DC bias voltage and the reflected RF power. Etch rates of between 4.77 – 21.52 nm/min have been achieved, with the higher etch rates being when the pressure and flow were low and the power was high (test 6). However, the same pressure and power has been used in test 5 with the only difference being the flow was higher in test 5. A higher flow can lead to a polymer build-up on the surface of Si [80], which will stop the plasma from reaching the surface, which will slow down the speed of the etch.

It has been observed that the etch depth around the smaller of the Al dots was greater.

The etch rates have been calculated from the average of the heights of the profile measurements of each dot on each sample, minus the thickness of the Al, and then the average height of the samples used in each test averaged to give the average etch depth for each test. The average height for each test has been divided by etch time of 60 minutes to give the average etch rates per test.

Test No.	Sample No's	Etch rate (nm/min)	DC Bias (V)	Reflected Power (W)
1	3,4,5	4.77 - 7.58	Not recorded	Not recorded
2	6,7	7.45 - 10.79	Not recorded	2.5
3	8,9	12.54 - 14.59	110	2.7
4	10,11,12,13	12.19 - 16.69	130	3
5	14,15	17.99 - 19.56	140	2.6
6	16,17,18	20.57 - 21.52	190	1.5

Table 6-3 - 100% CF_4 Si Etching results

Figure 6-4 below shows the step profile from dot 9 on sample 18 after etching, as can be seen the overall depth is approximately 13.8 KÅ (1,380 nm), which includes the Al. From the profile the deposited Al can be seen at point A where there is a change in the profile, and this has a height of approximately 1.54 KÅ (154 nm), thus making the etch depth of approximately 12.39 KÅ (1,239 nm).

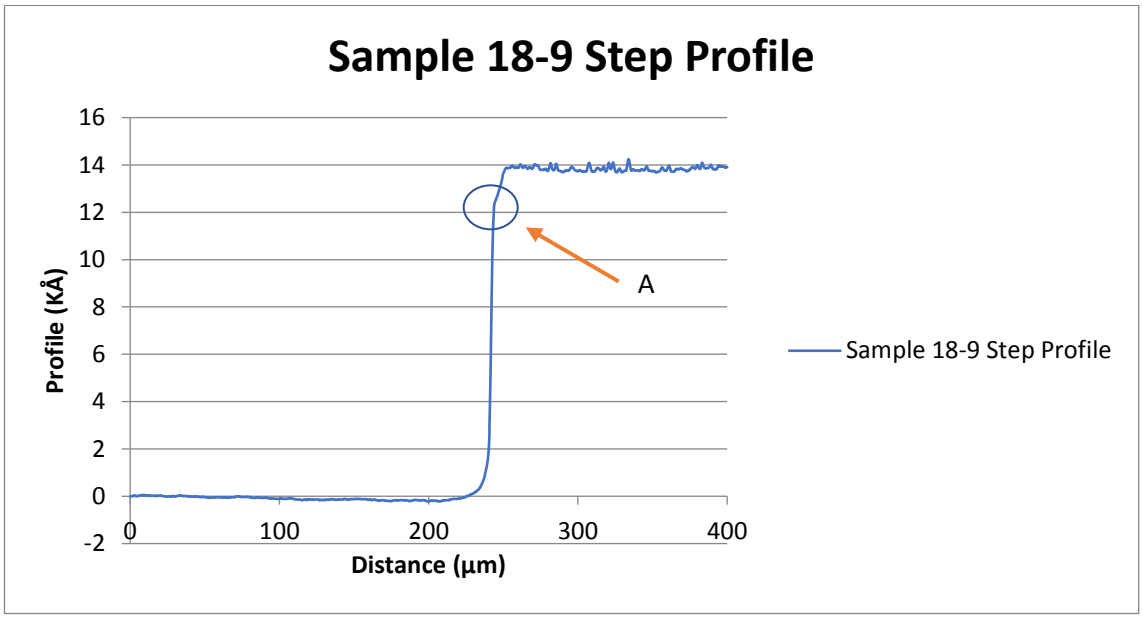

Figure 6-4 - Profile of sample after etching showing a Si etch depth of approximately 1.2µm up to point A and Al thickness of approximately 170nm from point A to the top

Profile measurements for checking surface damage of the etched Si have been carried out, with 8 sets of readings as before the etching. The average surface roughness calculated for sample 3 being 0.354 nm. This compares very well with the initial measurement of 0.443 nm, and is slightly less than the initial reading

taken, which indicates that no damage has been caused by the etching process and in fact the surface is smoother afterwards.

Figure 6-5 below shows an SEM image of one of the samples that has been etched in CF_4, interestingly the profile is indicating that the etch is slightly deeper next to the Al mask, which is called a mircotrench, where the area at the base of the mask has more ions due to the reflection off the side wall of the mask, which leads to faster etching in this area, as discussed by Moekstra et al [88].

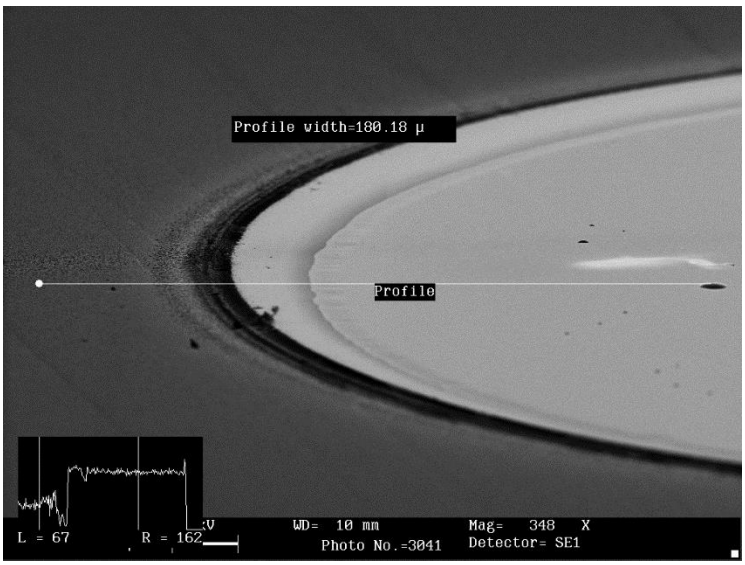

Figure 6-5 - SEM Image of CF_4 etching with an Al mask. Profile insert is showing a larger etch depth (Microtrench) around the Al base

6.6 CF_4 Photoresist etching

In addition to the tests carried out with the Al mask, which looked favourable, a number of tests were carried out etching Si in 100% CF_4 gas with a photoresist mask. Figure 6-6 below shows the etch profile of a pillar diode sample that has been prepared with a photoresist mask, and etched in 100% CF_4 for 2 hours at an RF power of 250W, assuming an etch rate of 21 nm/min as shown above with the Al mask tests, an etch depth of approximately 2,520 nm should have been possible, as can be seen from the profile the maximum etch depth is approximately 3,300 Å (330 nm). The initial photoresist was approximately 580 nm in thickness, hence this would give a photoresist selectivity of approximately 1.75 (580 nm / 330 nm) which agrees with the findings of Balachova et al [86].

Hence the photoresist would need to be 1.75 times thicker than the etch depth required. Selectivity being the different etch rates of different materials [68].

Figure 6-6 - CF_4 Photoresist pillar etch

6.6.1 CF_4 Photoresist Etching Electrical Characteristics

Some I-V tests have been carried out on the diodes which have been etched with 100% CF_4, with some good results obtained. Figure 6-7 below gives an example of an I-V curve for PR14. The turn on voltage is relatively high on this diode due to the high resistivity of the substrate used. PR14 is a pillar constructed diode with pillars of approximately 120 nm in height, with an annealed Al ohmic contact and Al Schottky contact, constructed on a p-type <100> substrate of 25mm x 25mm in size.

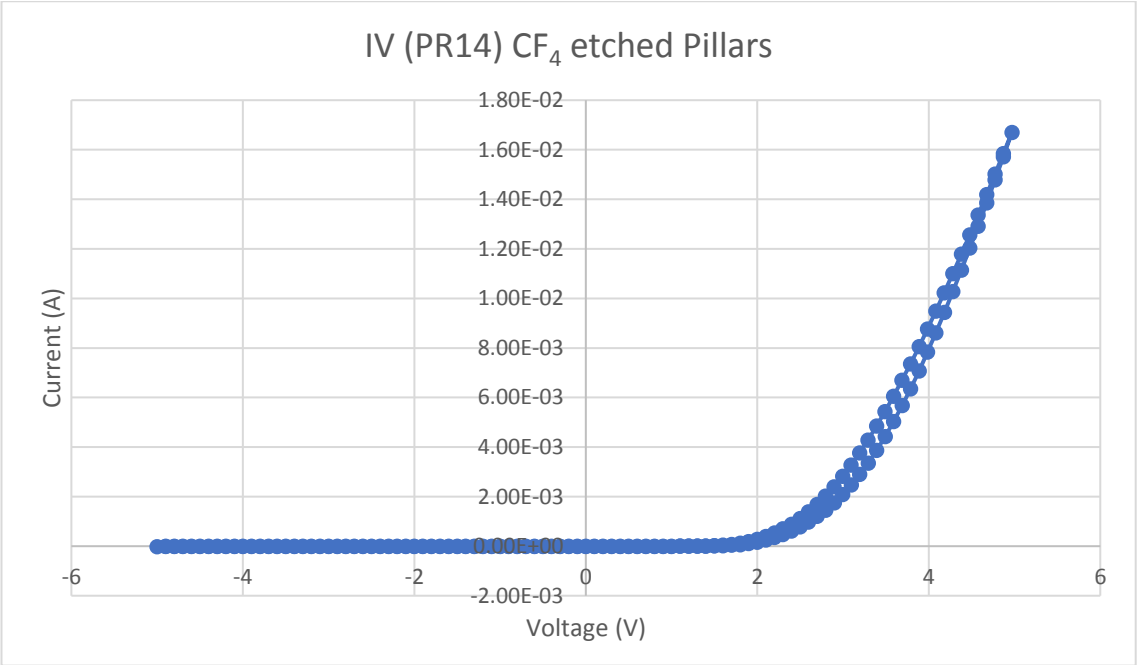

Figure 6-7 - IV Curve of PR14 CF_4 etched pillars

With reference to chapter 3, Table 6-4 below details the rectification ratio, and Table 6-5 the ideality factor for the diode depicted in Figure 6-7 above. The rectification ratio being good and ideality factor being in a range that has been reported before by Park et al [26]. The relatively high ideality factor is most likely due to an insulating interfacial layer, between the contacts and the Si which is known to cause high ideality factors as reported by Kim et al [48].

PR14 - Rectification Ratio			
Diode No.	Pillar Diode		
	Current (A) @		Ratio
	-1V	+1v	
	-7.01E-06	7.84E-03	3.05

Table 6-4 - PR14 Rectification ratio

PR14				
Pillar Diode				
V1	V2	J1	J2	η
4.28	4.97	1.03E-02	1.67E-01	**9.54**

Table 6-5 - PR14 Ideality factor

6.6.2 CF_4 Photoresist Etching Temperature Tests

Temperature tests have been carried out on some of the diodes which have been produced by 100% CF_4 etching, but these results were not conclusive and seemed to be random. It has been concluded that the results were not very good

due to the etch depth that has been achieved with 100% CF_4 etching, the pillar and solid constructed devices being too closely matched to observe any difference in temperature. The temperature tests have been carried out as detailed in section 5.2.

6.7 Conclusion

The results clearly show that etching of Si with 100% CF_4 is possible, and it is possible to produce a Schottky diode with good characteristics, however the etch rate is slow compared to etching Si with a mixture of CF_4 with O_2 [82] and wet chemical etching with something like KOH, where KOH etch rates are in the region of 1000nm/min [69]. Figure 6-8 below shows an optical image of a 100% CF_4 etched pillar diode with the Al top contact deposited, this has been slightly tilted to give an indication of the etch depth.

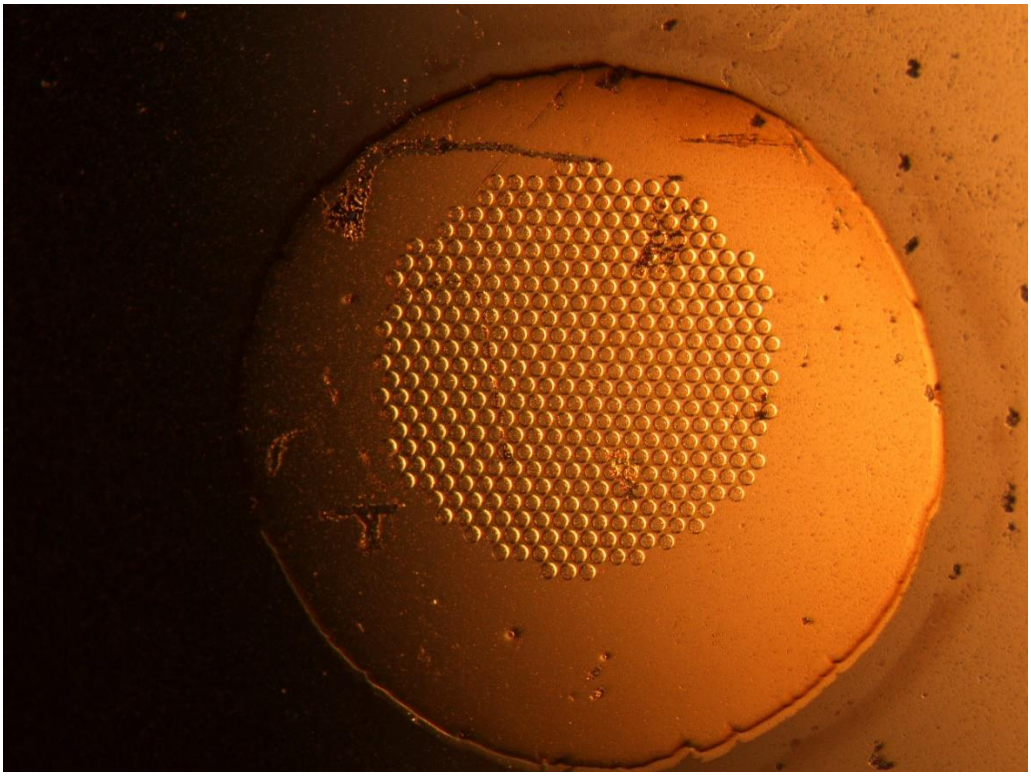

Figure 6-8 - 100% CF_4 Si Etched pillar diode optical image

If a small controlled etch depth is required, then this method would be suitable, as from the results it can be seen that the highest etch depth was achieved with a low flow of CF_4 and a higher power. The higher power gives more energy to the

ions and increases the physical etching process, the low flow of CF_4 avoids a polymer build-up on the surface of the Si [80], which can stop the plasma from reaching the surface and hence slowing down the speed of the etch.

The profile measurements of the Si surface before etching giving an average surface roughness of 0.443nm, and those of the surface after etching giving an average surface roughness of 0.354nm, showing that there is not much damaged caused to the surface of the wafer, and the wafer is smoother after etching.

Chapter 7 **Optimisation of using Wet Chemical (KOH) Etching**

7.1 **Introduction**

Wet chemical etching has been used for many years, where the object to be etched is submerged into a chemical solution, which is usually heated up for a prescribed time for the amount of etching that is required. To produce features on the objects some kind of mask is required, to protect the areas which do not want to be etched, and therefore this mask needs to be such that it does not get etched away, or does, but at a very slow rate compared to the material that needs to be etched.

7.2 **KOH**

Wet chemical etching of Si with potassium hydroxide (KOH), with different concentrations of solution and temperature of the solution, have been long studied in literature by Williams [69], Westra [89] & Burham et al [90]. A <100> Si wafer with a concentration of 30% KOH in H_2O and at a temperature of 70 °C, Williams [91] reports an etch rate of 1,100 nm/min. Westra [89] reports an etch rate of ~1,000 nm/min at 95 °C, and Burham et al [90] reports an etch rate of 1,400 nm/min. Varying amounts but all in a similar area, with a range of 1,000 to 1,400 nm/min.

In addition, IPA (Isopropyl Alcohol) can be added to the solution, to smoothen the surface and to reduce the number of micro pipes [92], in this case micro pipes being pits caused by the etching process, however, reducing the overall etch rate. In addition, the use of an ultrasonic bath helps with the etch process by removing the H_2 bubbles from the surface, as discussed by Monteio et al [92] and Ko et al [93].

There are a number of calculators and graphs that can be found On-line at Leland Stanford junior [94], clean room [95] & J Electrochem [96], that can be used for estimating the etch depth with different concentrations and temperatures of KOH solution, and with a concentration of 30% and temperature of 70 °C with an etch rate of 0.74 µm/min, the Leland Stanford Junior calculator also allows the etch

rate to be calculated with a saturation of IPA, and this gives an etch rate of 0.66 µm/min.

The etch rates from the calculator are summarised in Table 7-1 below for a temperature of 60/70/80 °C and concentrations from 20% to 50%. It should be noted that KOH is usually supplied in a solid state, and needs to be dissolved in water, the concentrations are the percentage of KOH to H_2O by weight.

Concentration (%)	Etch rate µm/hour Temperature (° C)			IPA Saturated @ 70 °C
	60	70	80	
20	26.57	48.60	85.92	
25	25.77	47.14	83.33	
30	24.30	44.45	78.59	39.61
35	22.29	40.79	72.10	
40	19.87	36.36	64.27	
45	17.16	31.39	55.50	
50	14.29	26.14	46.21	

Table 7-1 - KOH Etching rates for concentrations of 20 – 50% and temperature of 60 – 80 °C

7.3 Mask

Initially a negative photoresist mask was used, however, some of the first etching that was carried out suggested that the photoresist was being etched away. Due to the etch time being 30 minutes, and only having 5um spacing between pillars, which would result in the pillars being almost etched away, and giving the impression that the photoresist had been etched away. Figure 7-1 below shows an SEM image of sample PR68 which has been etched in KOH for 30 minutes, as can be seen the pillars are of a random size and some of them are very small, Figure 7-2 below also shows an SEM image of the undercutting that has occurred, with the pillars having a plateau on top.

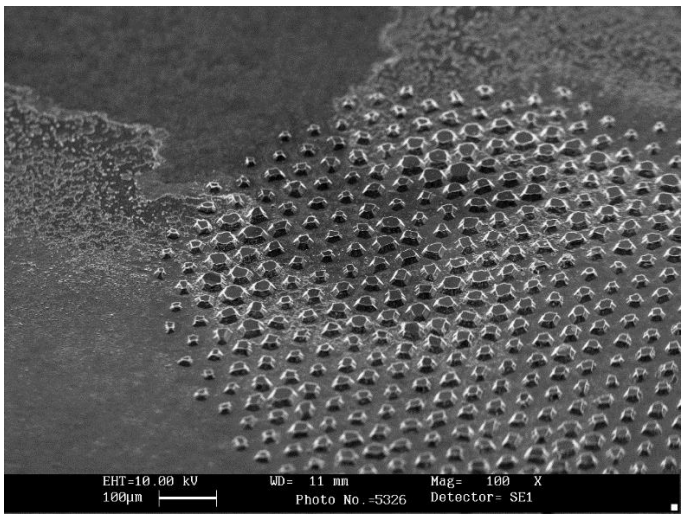

Figure 7-1 - PR68 Pillars SEM image after 30-minute KOH etch

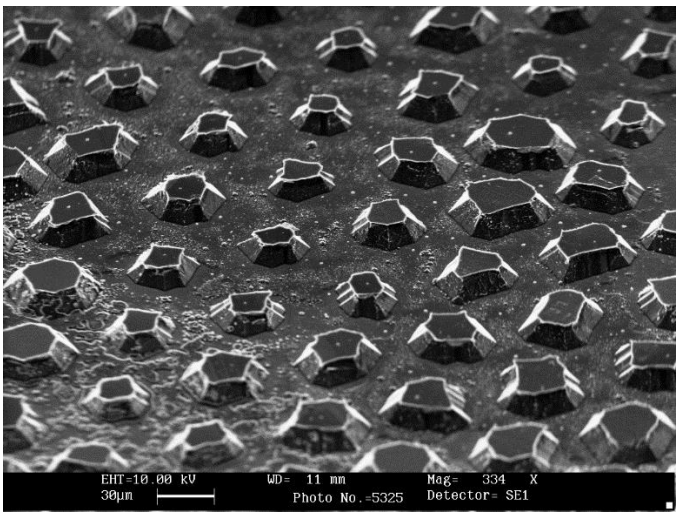

Figure 7-2 - PR68 KOH SEM image showing the KOH undercutting

The results provided in this thesis have been with a hard mask of SiNx, this mask has been produced with the aid of a photoresist mask and etching of the SiNx in CF_4, as detailed below. The hard mask being used due to having a slow etch rate in KOH solution, compared to the Si and will not be etched away.

7.4 SiNx Hard Mask

A hard mask of Silicon Nitride (SiNx) has been used as the KOH etchant mask, Williams [69] states that SiNx has an etch rate of 0.67 nm/minute in KOH, with a maximum etch time of 15 minutes it will require a minimum thickness of 10 nm of SiNx. With a proposed thickness of 60nm of SiNx to be used.

In addition to the resistance of SiNx to be etched in KOH, there is a need to be able to remove the SiNx once the Si etching has been carried out. Enmoto el al [97] reports that SiNx can be etched in CF_4 gas, with an etch rate of approximately 30 nm/min, Ohtake et al [98] reports an etch rate of 40 nm/min with 30W RF power but in a microwave etcher, in addition Reyes-betanzo et al [99] and Kastenmeier et al [100] report the etching of SiNx with a mixture of gases, which can achieve a higher etch rate, only CF_4 etching has been used in this research. A minimum etch time of 2 minutes would be required to etch the 60nm of SiNx, it is the intention to etch this for 5 mins to ensure that all of the SiNx has been removed, this may cause a small etch on the Si, but nothing detrimental.

SiNx is usually deposited in PECVD equipment, previously DMU have refined this process on the equipment at DMU, and Mih [78] PhD thesis provides the parameters to be used and gives an indication of the deposition time required for various thicknesses of SiNx.

7.5 Etching limitation

The mask that has been used for this research was designed to be used for etching with CF_4, and has gaps of 5µm between the pillars, CF_4 which gives anisotropy etching characteristic with a high aspect ratio in the downward direction, leading to not very much undercut. On the other hand, KOH etching also is anisotropy but has a lower aspect ratio and etches at an angle of 54.7 degrees in the <100> plane, with only having 5µm between the pillars this limits the depth of etch that can be achieved before serious undercutting occurs. Figure 7-3 below gives an overview of the KOH etching profile.

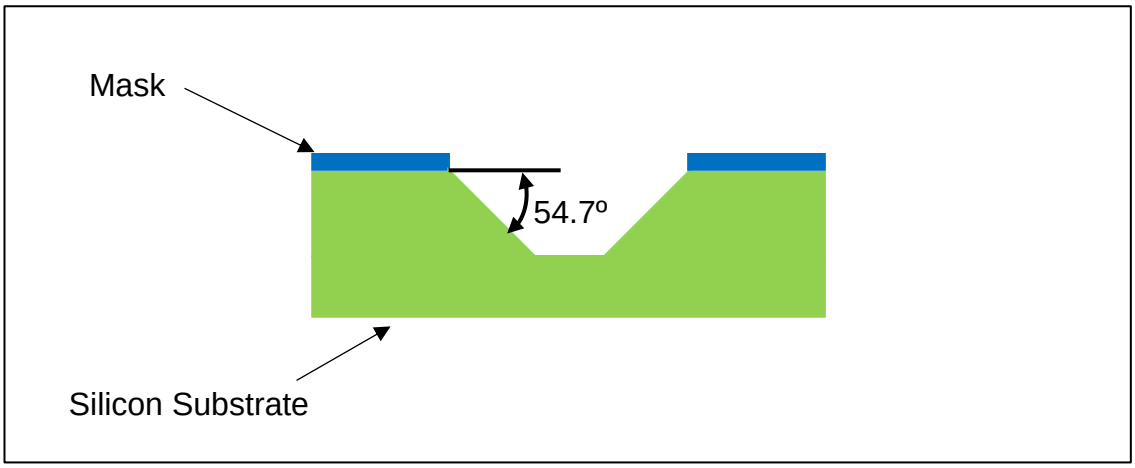

Figure 7-3 - Typical KOH etching profile diagram of 54.7°

Figure 7-4 below gives an indication of when the maximum etch depth would be achieved without serious undercutting of the mask, with a distance of 5µm between the photoresist. A simple bit of trigonometry would give a maximum etch depth of 3.53 µm as shown in Equation 7-1 below.

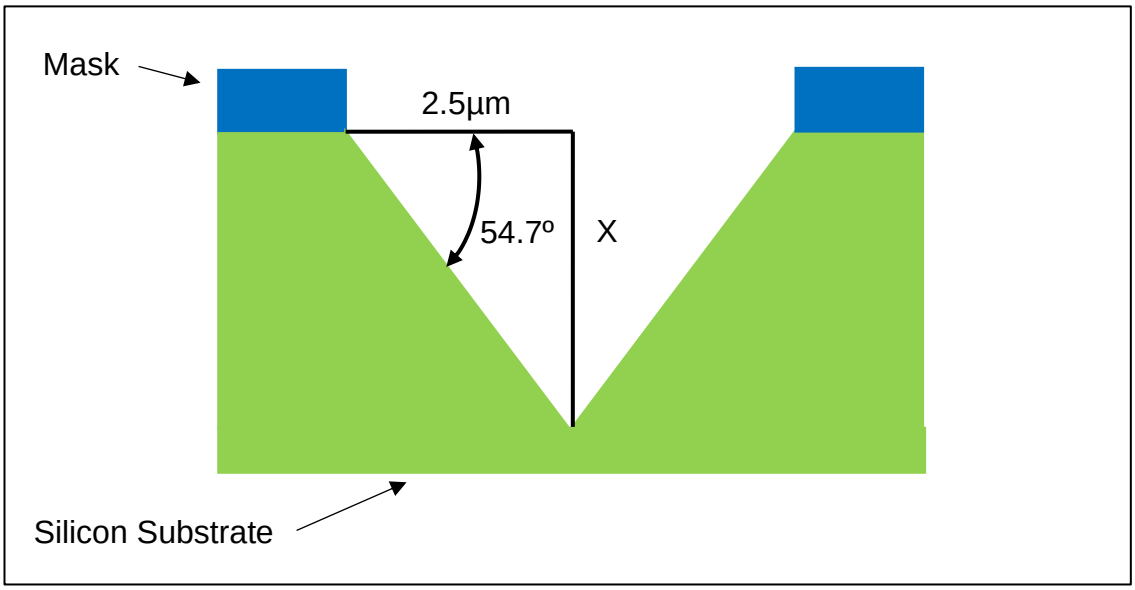

Figure 7-4 - Maximum KOH etch depth diagram with 5µm between features

$$X = tan^{-1}54.7 \times 2.5\mu m = 3.53\mu m \qquad \textbf{Equation 7-1}$$

From Table 7-1 above an etch depth of 3.53µm at 70 °C and 30 % concentration with no IPA would take approximately 4 minutes 45 seconds.

7.6 Etching results

The following etching results as shown in Table 7-2 below have been obtained, for 30% concentration and varying temperatures. The etch depth measurements were taken with a profilometer.

Sample	KOH concentration (%)	Temperature (° C)	Etch Time (minutes)	Etch Depth (µm)	Etch depth from table 7-1 (µm)
PR67	30	60	30	12	12.15
PR68	30	60	30	12.2	12.15
PR71	30	60	30	11.98	12.15
PR72	30	60	10	2.3	4.05
PR73	30	60	15	6	6.075
PR74	30	60	12.5	4	5.06
PR76	30	60	12.5	4	5.06
PR78	30	60	17.5	6.5	7.08
SD2	30	65.5	11.5	3.45	6.78
SD3	30	66.5	11	3.27	6.85
SD4	30	67	10.75	3.40	6.88
SD6	30	67.6	10	3.29	6.6
SD7	30	67.9	10	3.07	6.7

Table 7-2 - KOH Etching depth test results

Some of the results correlate quite well, but generally the etch depths obtained are lower than those as stated in Table 7-1 above. The KOH solution that was made up for the PR devices (PR67/68/71/72/73/74/76 & 78) was a smaller volume than the solution made up for the SD devices (SD2/3/4/6 & 7) and was made up at a different time, this could account for some of the difference in the two types of devices. In addition, KOH absorbs water from the atmosphere, and the solution may not have been exactly 30% by weight, but from Table 7-1 above 5% difference in concentration would only account for 3 µm/hour etch rate, which for a 10 minute etch time this would only account for approximately 0.5 µm reduction in the depth. The temperature measurements of the solution was of the

water surrounding the KOH, and not the KOH itself, as can be seen from Table 7-1 above the temperature has more of an effect on the etch rate, where a temperature of 10°C lower (70°C to 60°C) would give a 20 µm/hour reduction in the etch rate, for a 10 minute etch time this would be approximately 3.3 µm reduction in the etch depth, both of these could of affected the theoretical etch depth obtained.

7.7 **Other considerations**

It should be noted that Williams [69] states that evaporated Al will etch at a rate of 12,900 µm/minute. No figures are given for annealed Al, but it is assumed they will be similar. Due to the bottom Al contact being put onto the samples first, this would need to be thick enough to withstand a 15 minute etch, or be protected from the KOH. The thickness for a 15 minute etch would need to be 193 µm. This value is impractical to evaporate onto the samples and so the Al needs to be protected, or applied later on in the process, when the KOH etching has been completed.

Chapter 8 **Device Construction**

This Chapter describes how the Schottky diodes have been constructed and the processes that have been employed.

8.1 **Introduction**

The fabrication of the Schottky diodes has been carried out on a Si wafer, with 'P' type doping. Once the bottom Ohmic contact has been put onto the wafer, and this has been annealed, and a layer of Si Nitride (SiNx) has been deposited on the top polished surface, the wafer is cut up into small substrates, which are approximately 25mm x 25mm with a thickness of approximately 500µm. The substrates contain 16 Schottky diodes equally spaced on the substrate, half of the diodes are of solid construction (type A) the others are of pillar construction (type B). The devices have been produced using a top down approach. Figure 8-1 below gives a representation of the fabricated substrate.

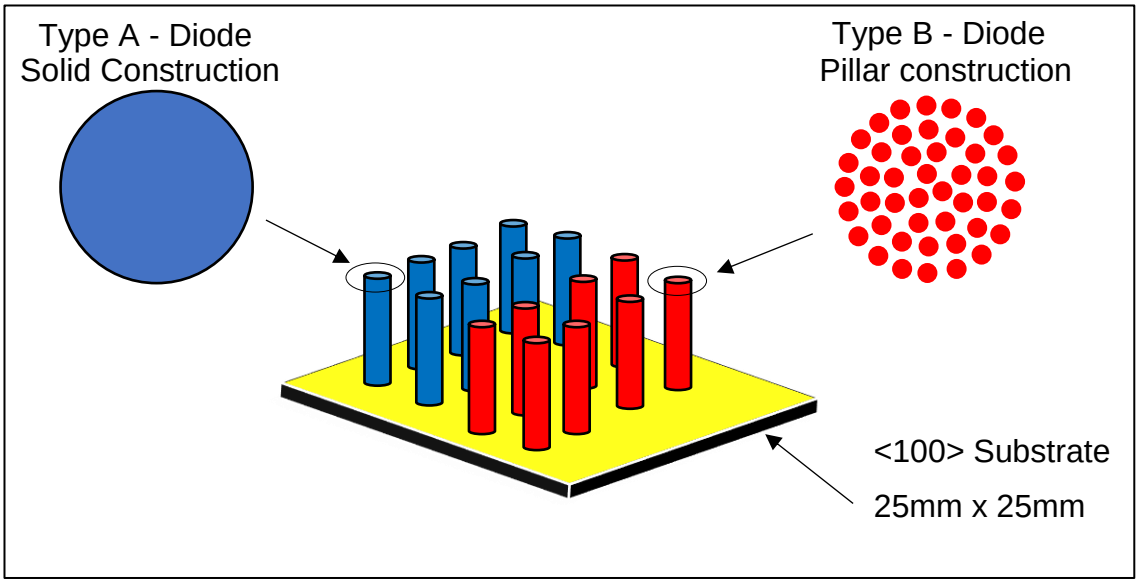

Figure 8-1 - Representation of the arrangement of the pillar and solid diodes on the substrate

There are several stages that are involved in the process to produce the devices, and to characterise the diodes, as shown in Figure 8-1 above. These processes are depicted in the process flow diagram in Figure 8-2 below. With type A and type B diodes being on the same substrate, they will be subjected to the same processes during the construction process.

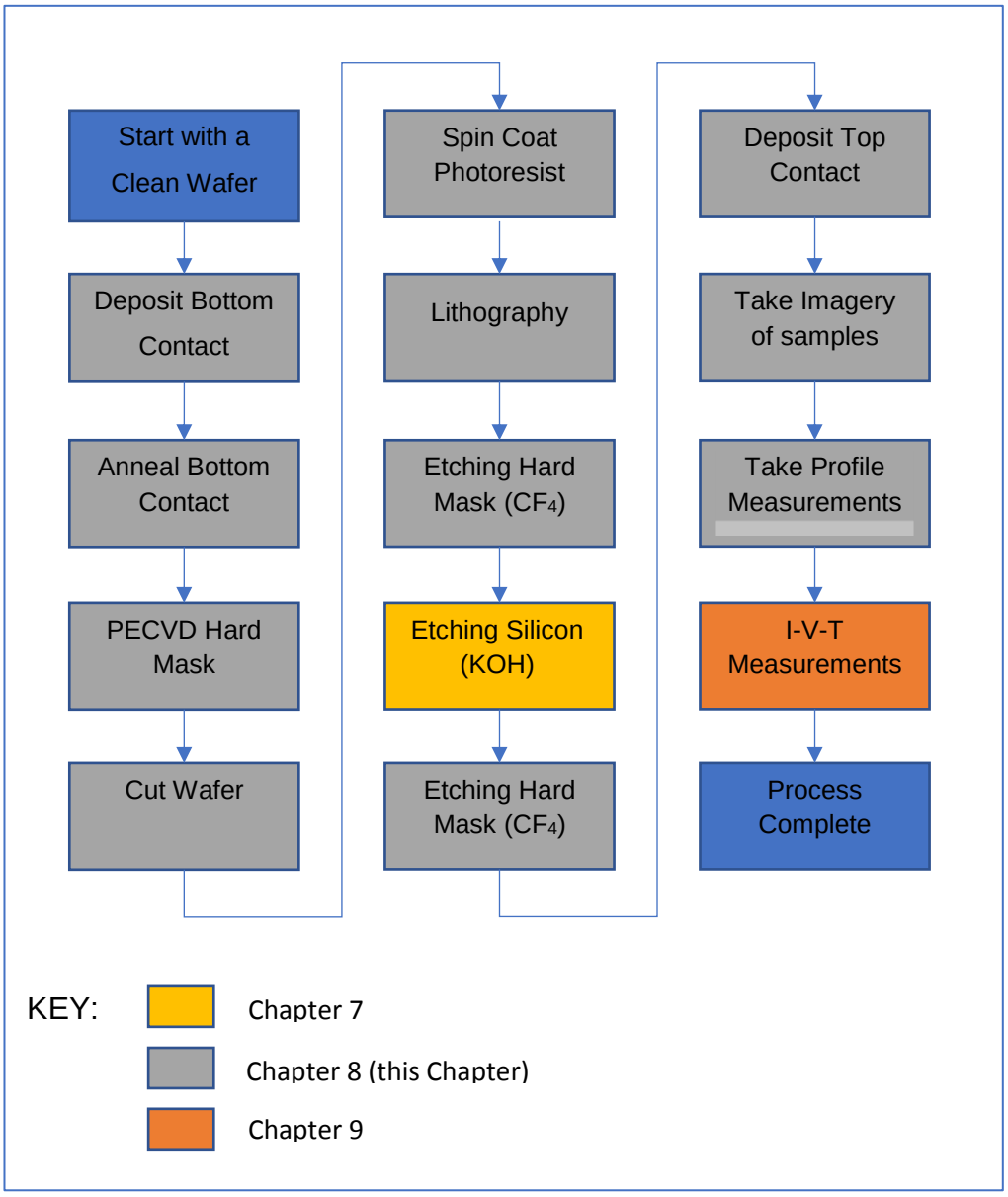

Figure 8-2 - Construction and measurement process diagram

To give a better understanding of how the devices are manufactured, the step by step process is shown in Figure 8-3 below. This shows a cross section of the substrate for a type B pillar diode, but the steps are also the same for the type A solid diode.

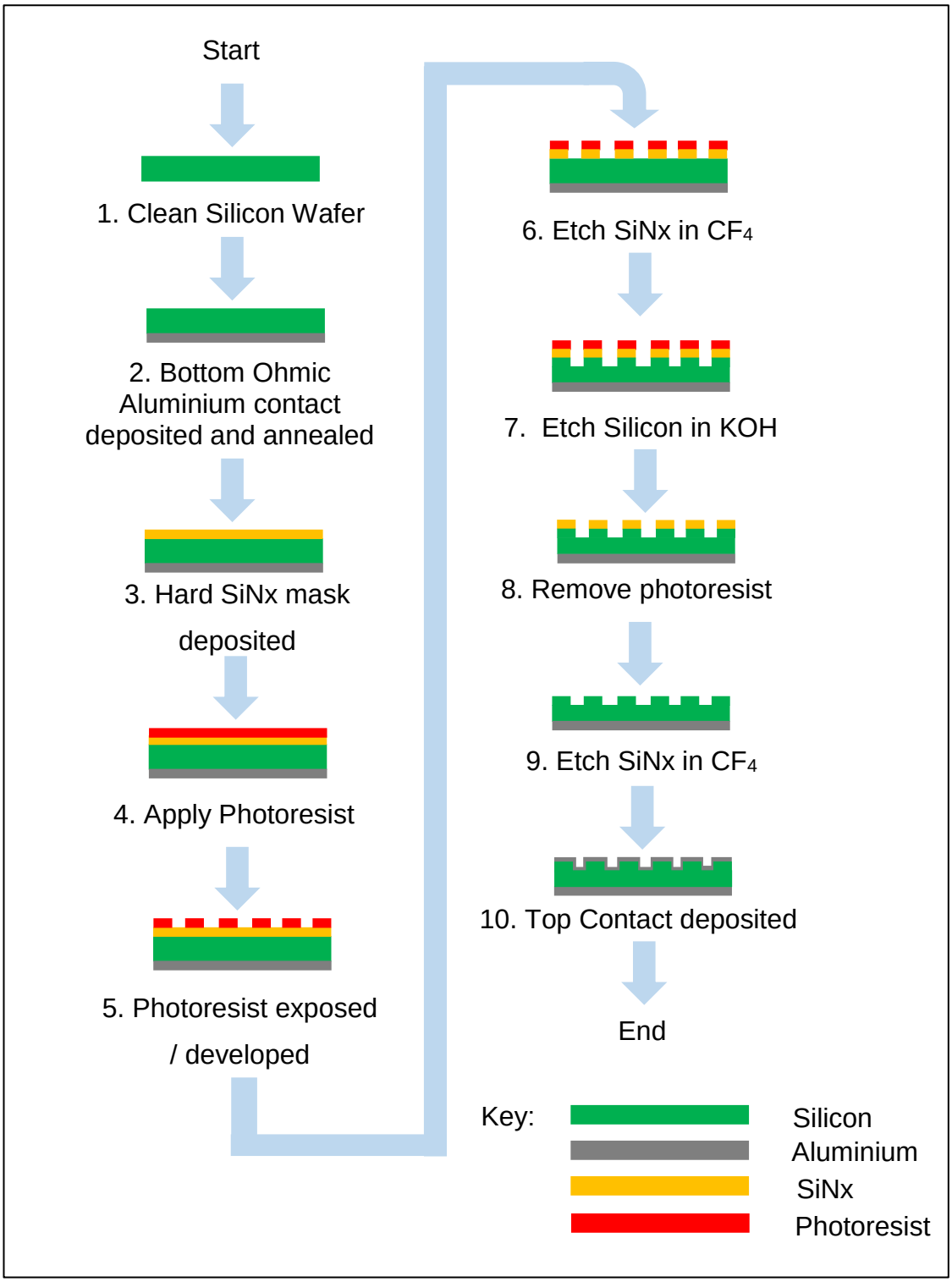

Figure 8-3 - Step by step manufacturing process diagram

The stages will be discussed further in more detail, with a description of the equipment utilised.

8.2 Deposition of top / bottom contacts

Deposition of the top and bottom Al contacts is performed by evaporation in a vacuum. The objective of the deposition process is to controllably transfer atoms from a heated source, to a substrate located a distance away, where film formation and growth proceed atomistically [101]. Thermal energy is imparted to atoms in a solid source, such that their temperature is raised to the point that they evaporate. The process is carried out in an evacuated chamber, with a very low pressure, in the region of 10^{-6} millibar. The Al is placed in a Tungsten wire basket, at the bottom of the chamber, and a current passed through it until the Al evaporates. For Al this is approximately 1000 °C [101]. When the Al makes contact with material, due to the lower temperature of the material, the Al will condense to form a thin film.

The area of the material to be deposited on is defined by a shadow mask, which is placed in close contact with the material, allowing predefined patterns to be deposited onto the surface.

A thickness monitor is part of the equipment, and is used during the evaporation process to assess how much Al has been deposited, and the rate of deposition, 1 nm/sec providing the best results and the best quality contact. The thickness monitor is used to stop the process when the required thickness has been achieved. The equipment that has been used is an Edwards Auto 306 as shown in Figure 8-4 below.

Figure 8-4 - Edwards Auto 306 evaporator

The evaporator has been used to deposit Al onto the Si substrates to form the two contacts for the Schottky diode. The contacts are applied at different times in the construction process for the devices. The bottom contact, which is the ohmic contact is deposited on the non-polished side of the wafer at the start of the process. A large shadow mask is used so that nearly all of the wafer surface can be covered with a thickness of 100 - 200nm.

The top contact, which will be the Schottky contact, is deposited onto the substrate as the last part of the process. For this a shadow mask is used, and will provide 2mm diameter dots on the surface of the substrate, positioned so that they align with the features on the surface. Again a thickness of 100 - 200nm is applied.

Figure 8-5 below shows the shadow mask that has been manufactured for the top contact, this is made from stainless steel with a thickness of 0.5mm.

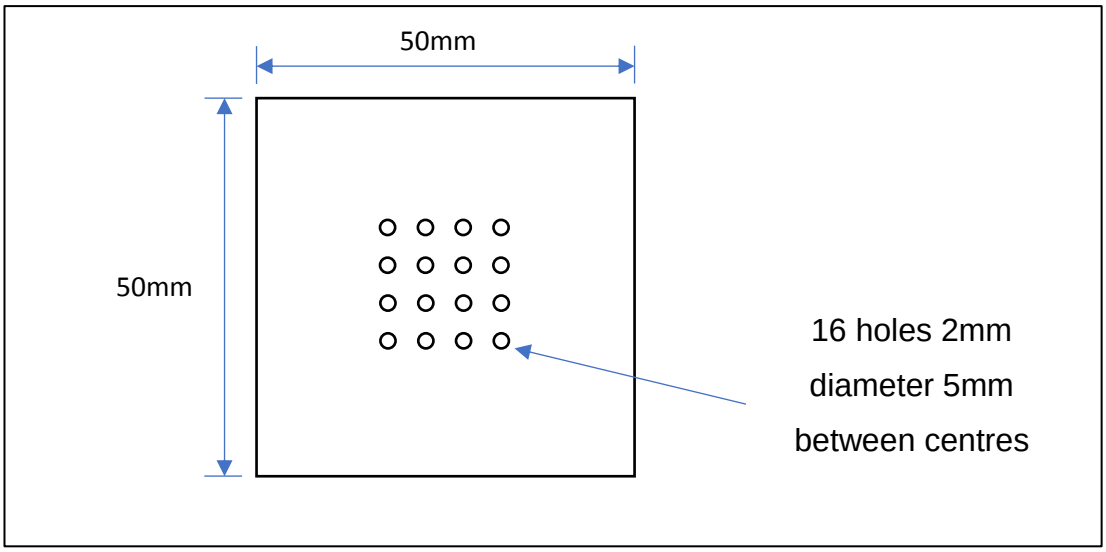

Figure 8-5 - Top contact deposition shadow mask

8.3 Annealing

Annealing is the process of heating materials up, to their eutectic temperature, to diffuse the materials together. In the production of a Schottky diode, this method is used to provide the low resistance ohmic contact. Annealing with Al will heavily dope the Si, and make it p-type as it is a trivalent atom, creating a hole. This will increase the tunnelling probability, therefore to provide a good ohmic contact for Al-Si bottom contact, this should be annealed around 450 °C.

The annealing process has been used to provide the bottom ohmic contact for the Schottky diodes.

The equipment that has been used for the annealing process is a Carbolite vertical furnace, as shown in Figure 8-6 below, and the control unit is shown in Figure 8-7 below.

Figure 8-6 - Carbolite vertical furnace photo

Figure 8-7 - Carbolite vertical furnace controller photo

The samples are stacked on a quartz holder, which are then placed into the furnace, and drawn up into the chamber before the heating cycle. The furnace chamber is purged with N_2 at a flow rate of 2 litres / min for 10 minutes. The N_2 flow is then reduced by half. The heating cycle is then commenced, and when complete the furnace is left to cool down before removing the samples. The cooling down of the chamber is by natural convection. Once cooled down sufficiently the N_2 is turned off and the samples are withdrawn from the chamber and removed.

The heating cycle used is:

- Ramp the temperature up to 500 °C at a rate of 20 °C / minute
- Hold the temperature at 500 °C for 30 minutes
- Naturally cooling down to room temperature, from 500 °C to 25 °C takes approximately 7 hours

500 °C is used to allow for any tolerances in the test equipment, to ensure that the annealing is carried out above the eutectic temperature of the Al.

8.4 Wafer Cutting

As discussed above the substrates are cut from a Si wafer of approximately 100 mm in diameter. These wafers are relatively easy to cut, and usually cut in a straight line. A diamond tipped scribe is used to nick the edge of the wafer, where required, and the wafer can easily be cut into 25mm squares.

8.5 PECVD (Hard Mask)

Plasma Enhanced Chemical Vapour Deposition (PECVD) is a process where thin films can be deposited on the surface of a substrate, by chemically reacting a volatile compound of a material to be deposited, with other gases, to produce a non-volatile solid that deposits atomistically on the surface of the substrate [101]. Within a chamber at very low atmospheric pressures and varying temperatures. The chemical reactions occurring after creation of a plasma of the reacting gases using an RF 13.56MHz source [68], the plasma allowing the chemical reactions to take place at a lower temperature than conventional Chemical Vapour Deposition (CVD) process. The film to be deposited is defined by the mixture of

and concentrations of the gases used, and the thickness determined by the reaction time used.

The equipment that has been used for the hard mask is made by Plasma technology as shown in Figure 8-8 below, this is a parallel plate reactor.

Figure 8-8 - Plasmalab PECVD equipment photo

The PECVD system has been used to provide a hard mask of Silicon Nitride (SiNx), a hard mask is required to withstand the etching process with KOH. The process of applying SiNx has been refined by previous research students at De Montfort University (Thomas Attia Mih, PhD 2011) [78]. Table 8-1 below details the PECVD parameters for the deposition and Table 8-2 along with Figure 8-9 below give the approximate thickness of SiNx deposited for RF energisation time.

PECVD settings for SiNx Deposition	
Pressure (mTorr)	350
Temperature (° C)	300
RF Power (W)	20
SiH_4 (sccm)	6.6
NH_3 (sccm)	40
N_2 (sccm)	100

Table 8-1 - PECVD deposition conditions of SiNx.

SiNx Deposition Thickness	
Time (minutes)	Thickness (nm)
1	13.8
5	30
10	60
20	110

Table 8-2 - SiNx Thickness vs deposition time

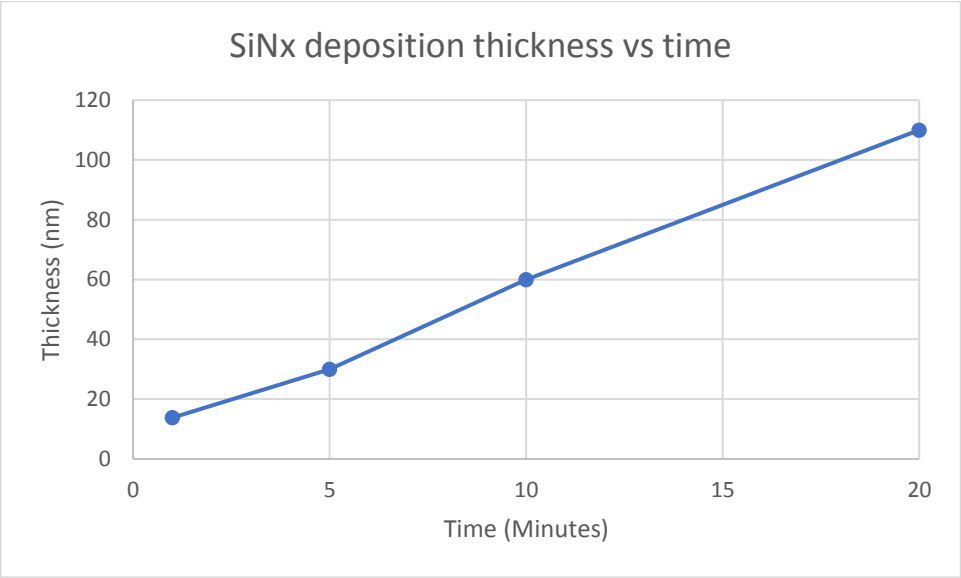

Figure 8-9 - PECVD SiNx deposition thickness vs time graph

Due to changes in the PECVD equipment it is not possible to set the same flow parameters for SiH_4 and NH_3 as detailed in Table 8-1 above, the parameters that have been used are detailed in Table 8-3 below. These are not dissimilar to the original figures but will give a slightly different thickness of SiNx for the same deposition time.

PECVD settings for SiNx Deposition	
Pressure (mTorr)	350
Temperature (° C)	300
RF Power (W)	20
SiH_4 (sccm)	10
NH_3 (sccm)	90
N_2 (sccm)	100

Table 8-3 - Actual SiNx deposition conditions

Only a thin layer of SiNx is required, the etch rate of SiNx in KOH is very low in the region of 0.67 nm per minute [69]. The etch times will be up to 15 minutes, so a SiNx thickness of above 10 nm is required, to ensure that an ample layer of SiNx is deposited, the RF energisation will be on for 10 minutes, which gives a thickness of approximately 60 nm.

Some tests have been carried out, to ensure that the thickness of SiNx could be obtained with the new parameters. Two RF energisation times of 5 and 10 minutes were used, and the results are shown in Table 8-4 below.

SiNx Deposition Thickness			
Time (minutes)	Thickness (nm)		
	Sample 1	Sample 2	Average
5	37.9	38.0	37.95
10	68.2	66.1	67.15

Table 8-4 - SiNx PECVD thickness test results

The thickness of the SiNx was measured with an Ellipsometer, as can be seen with the new parameters a slightly thicker layer of SiNx is deposited.

8.6 **Spin Coating**

Spin coating is a method used to apply a liquid onto the surface of a substrate, to allow an even distribution of the liquid, and to control the thickness of the liquid on the surface. The liquid can be applied when the material is static or when it is dynamic (spinning). The system allows a number of different steps to be programmed per cycle, with different ramp and dwell times, according to what is required, a typical cycle would be.

- Application step
- Dispersion Step
- Spreading step
- Drying step

The application step can be static or a slow spin speed. The dispersion step will be a slow spin speed to spread the liquid over the surface. The spreading step will be a high-speed spin, this will determine the final thickness of film on the

surface, and the drying step will be a slower speed, or the same as the spreading speed, in order to allow the liquid to dry on the surface.

The system is used by placing the substrate onto the plate, which is held in place by a vacuum, and the chosen spin cycle is started.

The spin coater has been used to apply the photoresist to the samples whilst static.

The spin coater that has been used is a G3P Spincoat manufactured by Speciality Coating Systems, as shown in Figure 8-10 below.

Figure 8-10 - G3P Spin coater used for depositing photoresist

8.7 Lithography

Lithography in general terms is the process of applying ink to a material, which ends up with the ink only in the places that are required. The ink adheres to parts of the surface, and by the application of a substance that the ink will not stick to on the surface, it is possible to create intricate patterns on the surface.

To define the patterns when using photoresist, the photoresist needs to be exposed to an Ultra Violet (UV) light source. This is achieved with the aid of a mask. The mask is placed over the top of the sample, which has been covered in photoresist. This is then exposed to the UV light, which allows parts of the photoresist to be removed, as part of the development photoresist process.

Lithography has been used to define the areas of the samples that don't want to be etched away.

The UV light source used is a Kasper Mask Aligner as shown in Figure 8-11 below.

Figure 8-11 - Kasper mask aligner UV light source photo

The Kasper mask aligner is only being used as a UV source, with the mask placed manually onto the sample.

The UV source is turned on for 20 minutes, the sample and mask are placed beneath the UV source, and the shutter is opened manually between 2 and 10 seconds.

8.8 Lithography Mask

The etching process requires a photoresist to be applied to the substrate, so to facilitate this a mask is required for the exposure part of the photoresist application process.

A 5" x 5" chrome on glass mask was produced by a company called "micro Lithography Services Ltd". This was produced from the .dxf drawing file that had been produced on the AutoCAD ® drawing package. Three different images have been produced on the same mask, as discussed above. Half are solid and are

the same on all three images, and these are 1mm diameter dots. The other half have the following characteristics;

- 400 50µm dots
- 625 40µm dots
- 1111 30µm dots

The above dots are all clustered together in a circle with 5µm spacing between the dots. The size and number of dots have been calculated to give the same volume of Si as the 1mm diameter dots, once etched. The calculations are as below.

With the assumption that the etch depth is the same in this instance i.e. 2 µm the volume of the 1mm diameter dots will be;

$V = \pi * r^2 * h$

Where;

r is the radius = 1/1000/2 m and
h is the etch depth = 2/1000000 m
$\therefore V = \pi * 0.0005^2 * 0.000002 = 1.57e - 12m^3$

And the volume of the clustered dots will be;

$V = \pi * r^2 * h * n$

Where;

r is the radius = 50/1000000/2 m or 40/1000000/2 m or 30/100000/2m
h is the etch depth = 2/1000000 m and
n is the number of clustered dots = 400 or 625 or 1111

$\therefore V = \pi * 0.000025^2 * 0.000002 * 400 = 1.57e - 12\ m^3$ for the cluster of 400 dots

$\therefore V = \pi * 0.00002^2 * 0.000002 * 625 = 1.57e - 12m^3$ for the cluster of 625 dots

$\therefore V = \pi * 0.000015^2 * 0.000002 * 1111 = 1.57e - 12m^3$ for the cluster of 1111 dots

There are two different types of photoresist which are available, “positive” and “negative”. A positive photoresist uses a mask that allows the UV source to expose the area that is not required, a negative photoresist uses a mask that allows the UV source to expose the areas that are required. The UV source degrades the positive photoresist, and the developer will remove this part, whereas the UV source strengthens the negative photoresist and allows the developer to remove the parts not exposed. After some research it was decided that a negative photoresist would be used, mainly because of the better adhesion characteristics, and the availability of the negative photoresist kit. A mask has been produced so that the areas that need to remain on the substrate will be exposed to the UV source.

Below Figure 8-12 is an overall image of the mask and Figure 8-13 is an image of one of the cluster of dots, the clear areas being those that will remain on the substrate.

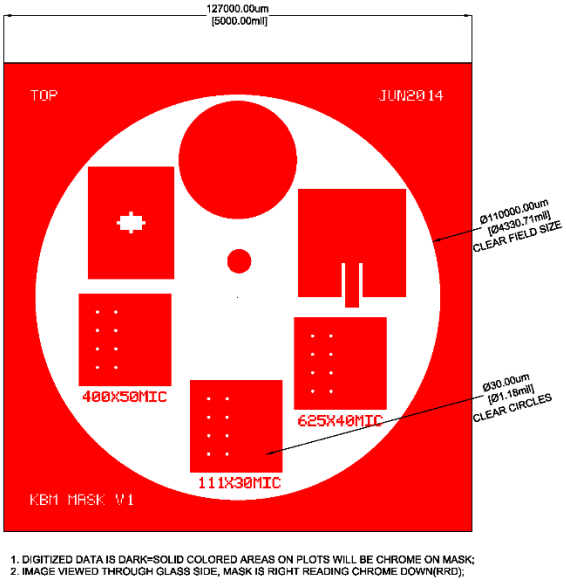

Figure 8-12 - Image of lithography overall mask

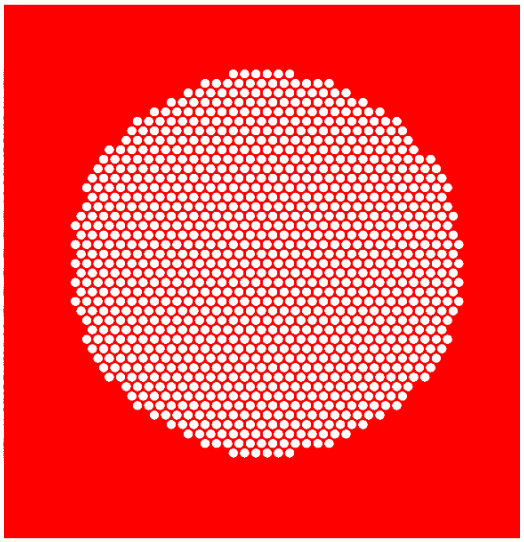

Figure 8-13 - Image of lithography cluster of dots

8.9 Photoresist

A Negative photoresist kit 1 (654892) was Purchased from Sigma-Aldrich. This contains the photoresist, thinners, developer and remover. The viscosity of the photoresist is relatively high, and to enable a good coverage of the surface of the substrates, this was diluted with the thinners at a ratio of 50/50. Spin coating was tried with the photoresist at 100% concentration, but not very good results were obtained, and a thick layer of photoresist was achieved. The photoresist is applied to the polished side of the substrate.

The photoresist application has been carried out by spin coating on a G3P Spincoat system, the following steps are involved which are detailed in Sigma Aldrich procedure [102];

- Cleaning
- Application
- Pre-bake
- Exposure
- Development
- Post bake

Each of the above are described in detail below.

8.9.1 Cleaning

The substrates are cleaned with several applications of IPA and dried with a N_2 gun and then placed on a hot plate for 20 minutes at a temperature of 120°C.

8.9.2 **Application**

After the cleaning process the photoresist is applied to the substrate. The substrate is placed in the spin coater, 1cl of diluted photoresist is placed onto the static substrate with a syringe, and then the spin cycle is started. The spin cycle consisted of two parts, the 1st spin rate to spread the photoresist out, and a 2nd spin rate to achieve the thickness required and dry the photoresist. The 1st spin was for a dwell time of 5 seconds with a ramp up rate of 1 second, the 2nd spin was for a dwell time of 60 seconds with a 1 second ramp up rate, as depicted in Figure 8-14 below.

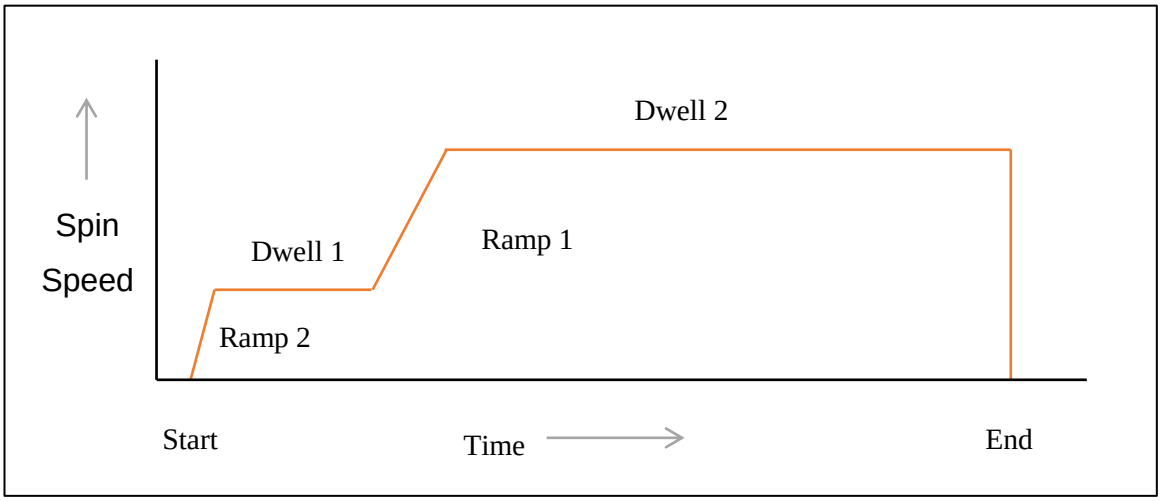

Figure 8-14 - Photoresist spin cycle steps

Various different spin strategies have been applied to gain the thickness of photoresist required. Table 8-5 below shows the spin strategies and the thickness of photoresist achieved. The thickness of the photoresist was measured on the Profilometer, after the photoresist had been exposed/developed, leaving only the photoresist where the diodes are to be formed. Two of each spin strategy was produced and measured.

Spin Strategy Number	Spin Parameters (rpm)		Average Photoresist Thickness achieved (nm)
	1st Spin	2nd Spin	
1	750	750	757
2	750	1000	649
3	750	1250	637
4	750	1500	556
5	750	1750	495
6	750	2000	501

Table 8-5 - Spin strategy step parameters

Figure 8-15 below gives a pictorial view of the photoresist thickness, where spin speeds of 1750 and 2000 rpm are not very much different. It can be seen from the trend line that the higher the spin speed the thinner the photoresist.

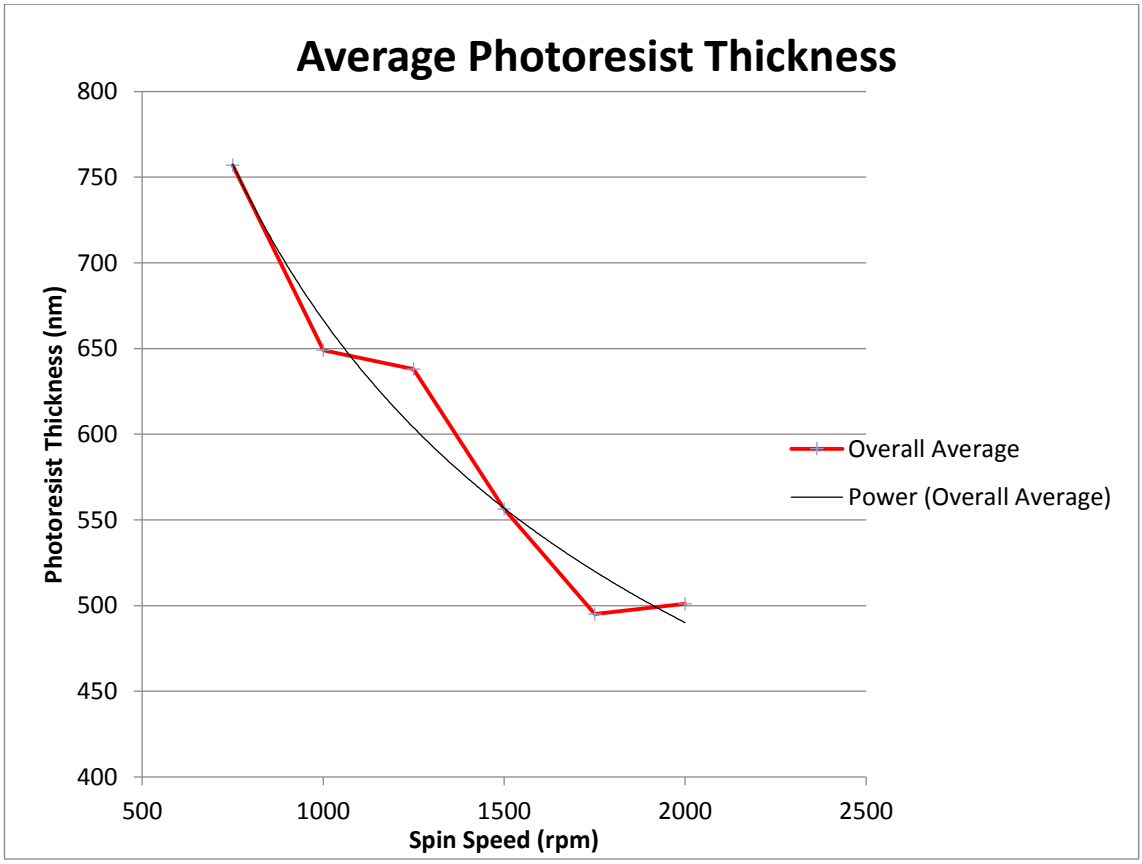

Figure 8-15 - Average photoresist thickness measured using a Tencor profilometer

The above graph correlates well with the general equation for spin coating thickness, which can be found on ossila.com web site [103] as shown in Equation 8-1 below, increasing the speed by four times halves the thickness.

$$t \propto \frac{1}{\sqrt{\omega}}$$

Equation 8-1

Where;

t is the thickness of the photoresist (nm)

ω is the angular velocity (Radians / Sec)

The thicker the layer of photoresist on the substrate, a longer etching process can be applied to achieve a higher etch depth. From images of the samples above, it was decided that the second spin rate of 750 rpm gave a better quality of photoresist, with the exposure and development process employed. Figure 8-16 below shows an optical image of one of the samples above.

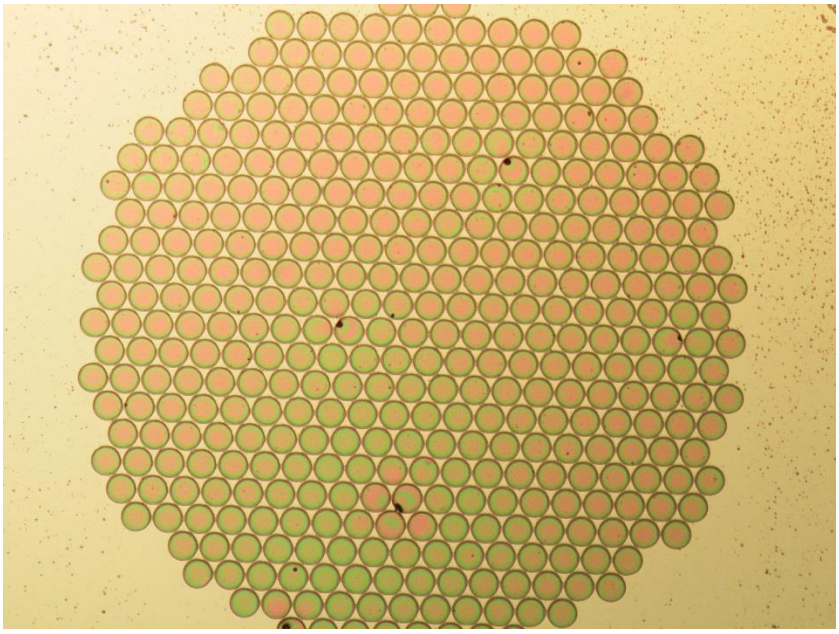

Figure 8-16 - Photoresist optical image of pillars

8.9.3 **Pre-Bake**

After the application of the photoresist the substrate is pre-baked on a hot plate at a temperature of 82°C for 20 minutes. This process gives additional adhesion

of the photoresist to the substrate, but still allowing the photoresist to be developed, and the parts that are not required to be removed.

8.9.4 **Exposure**

The substrate is then exposed with an Ultra Violet (UV) light source. This was carried out on a Kasper Mask Aligner. The supplier of the photoresist gives an indication of the exposure time of between 1 and 10 seconds, initially an exposure time of 6 seconds was used but this was causing the pillars definition to be poor, due to the light affecting more of the photoresist, as shown in Figure 8-17 below, where there are no gaps between the pillars. Several different times have been tried out, but an exposure of 2 seconds timed manually seems to give a good definition once developed, and this is the time that has been applied. Figure 8-18 below shows a photoresist image where the exposure time was two seconds, this clearly shows well defined pillars with gaps between the pillars.

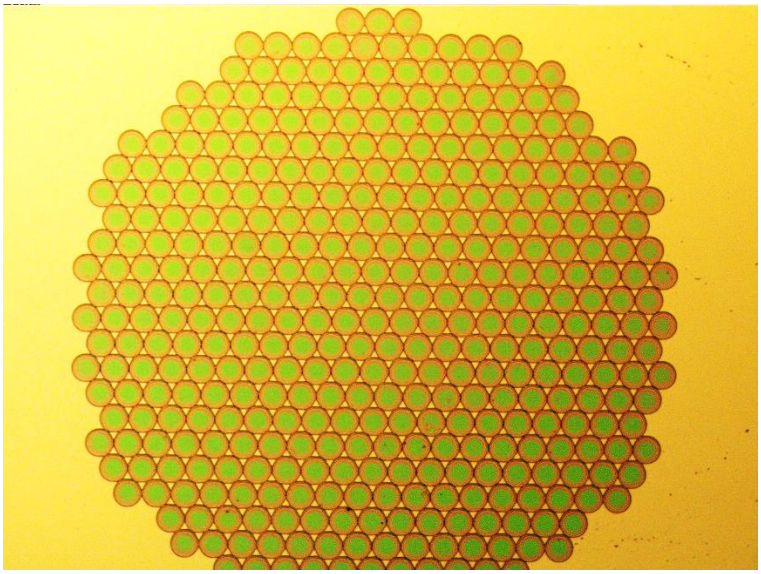

Figure 8-17 - Six second photoresist exposure optical image

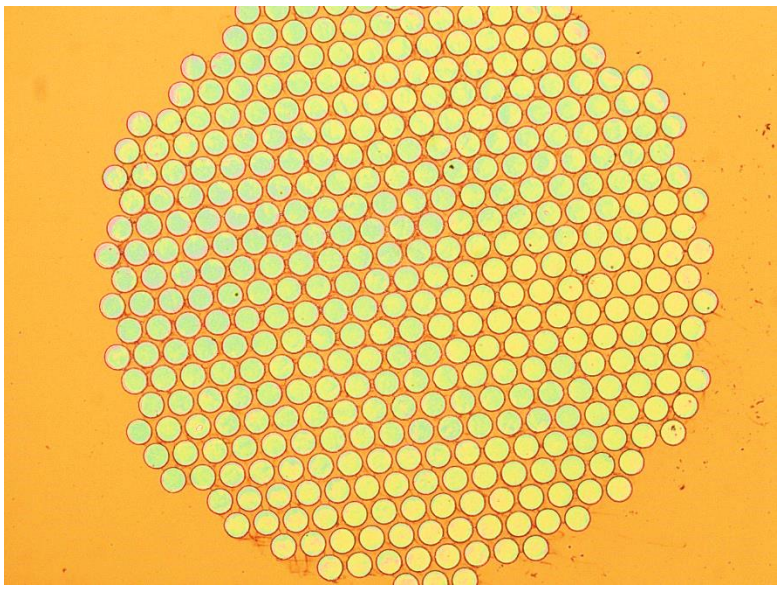

Figure 8-18 - SD2 Two second photoresist exposure optical image

The UV light source is allowed to warm up for 20 minutes before the exposure is applied so as to give a good constant light intensity. The substrate is placed on the Kasper Mask Aligner plate, and the mask is placed on top of the substrate manually giving a touch contact with the weight of the mask, this contact method was found to give a sharper photoresist of the correct size. Once positioned and the UV source warmed up, an exposure of 2 seconds is applied. Figure 8-11 below shows the Kasper Mask Aligner used.

Figure 8-19 - Kasper mask aligner photo

8.9.5 **Development**

Once exposed the photoresist is then developed, where the development process removes all of the photoresist which has not been exposed to the UV light source.

Several different methods of applying the developer have been tried out, i.e. spraying on, with a fine and course mist / spray, and dipping. Dipping has been found to be the most effective way of getting a good crisp application of photoresist. Dipping for more than about 30 seconds removes all of the photoresist. The method found to give the best results is as follows.

- 10 second dip
- Several rinses with IPA
- Quick in and out dip
- Rinse with IPA
- Quick in and out dip
- Several rinses with IPA

The quick in and out dips, for about one second, are mainly used to clean the excess photoresist off the surface of the substrate, as there seems to be a residual left over if this is not carried out. Figure 8-20 below shows the residue if the substrates are not dipped in and out a couple of times. However, this does mean that additional development is carried out, but the 10 seconds first dip has been reduced to account for this.

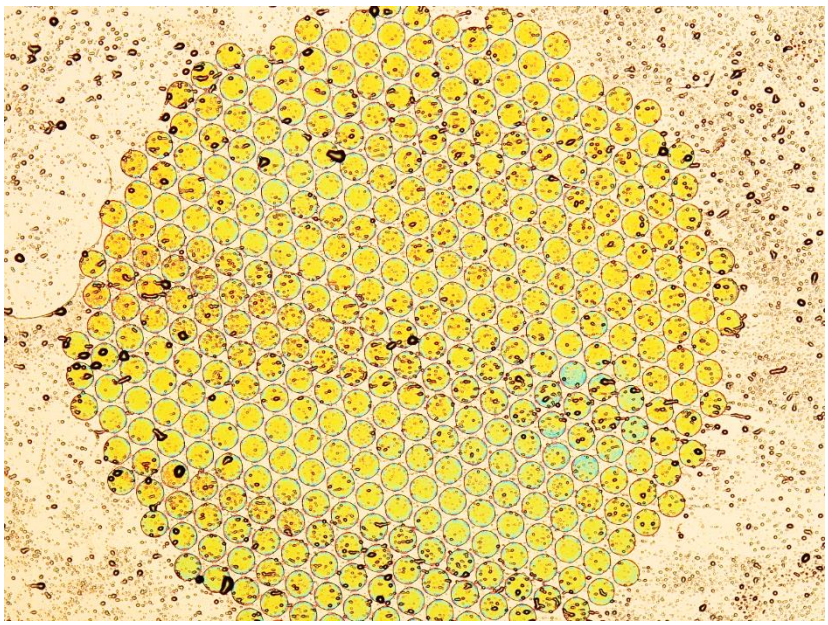

Figure 8-20 - Photoresist optical image showing debris on surface when not dipped

8.9.6 Post Bake

Once the substrates have been developed a post bake is carried out, on a hot plate, at a temperature of 120 °C for a period of 10 - 20 minutes. This process stabilises the photoresist, which is now ready to be etched.

8.10 Etching

This section details the dry etching of the SiNx and the wet chemical etching, which have been used in the manufacture of the devices.

8.10.1 Dry Etching SiNx

During the manufacturing process the SiNx needs to be removed, before the etching of the Si in KOH, and after the photoresist has been removed. Tatsuya et al [97] states that SiNx can be etched at 30 nm / minute in CF_4 gas at room temperature, the thickness of SiNx is approximately 60 nm on the samples produced. This would mean that an etch rate time of two minutes would remove all of the SiNx. For the first etching the etch time needs to be as short as possible so that the photoresist is not removed. If this is removed the SiNx beneath will also be removed, which is not desirable. From experiments undertaken it has been concluded that the photoresist will be removed in approximately 15 minutes, when etched in CF_4, and at an RF power of 200W. Therefore to ensure that the SiNx will all be removed, and the photoresist will remain, an etching time of 5

minutes will be used. For the second etch time there are no time constraints, and this will be etched in CF_4 for a duration of 10 minutes. The additional etching time will ensure that all of the SiNx has been removed, but it will also mean that the Si will be etched slightly. This etch rate is very low as detailed in chapter 6 and will not be an issue.

8.10.2 **Wet Etching**

The most common method of wet etching Si is by using a KOH solution. The KOH is purchased as a solid and is dissolved in water, at different ratio's to give different etch rates. The ratio that has been used is 30% KOH to water by weight. In addition to the mixture ratio, the temperature of the solution affects the etch rate. The higher the temperature the faster the etch rate. A solution temperature of 70 °C has been used. The ratio used, and temperature, gives an etch rate of approximately 1µm/minute.

8.11 **Ohmic & Schottky contact application**

A typical Schottky diode consists of an Ohmic and Schottky contact. For use with Si SZE et al [15] shows that Al can be used for both the Schottky and Ohmic contacts, the only difference being is that the Ohmic contact is made by annealing at a temperature of 500°C for 30 minutes. This then allows the metal to diffuse into the Si, thus creating a low resistance connection.

Firstly a layer of Al is deposited on the backside of the substrate, non-polished side, with a thickness of approximately 200nm. This is then annealed at 500°C, for 30 minutes to form the ohmic contact.

Secondly a layer of Al is deposited onto the top of the etched features only, by using a shadow mask, which has holes the size of the deposited material required (Schottky contact).

To allow access of the bottom ohmic contact for testing purposes, a piece of Al foil bigger than the substrate size is fixed to the ohmic contact with silver paste. The Al foil is then used for one of the measurement instrument contacts, the other contact is placed directly on the deposited Al Schottky top contact.

Figure 8-21 below shows an image of a prepared substrate ready for carrying out measurements.

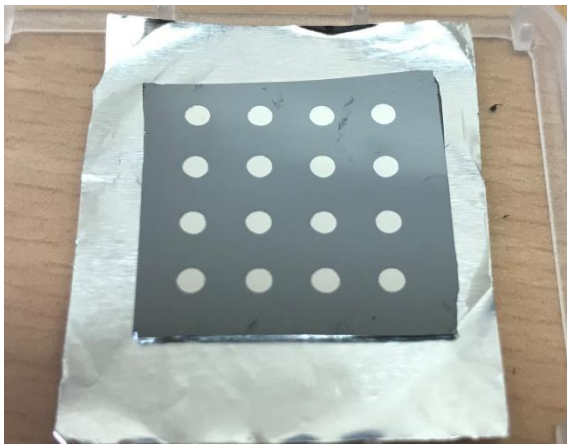

Figure 8-21 - Photo of a sample ready for testing

8.12 Test Diodes

From all of the diodes which have been produced, five of the latest substrates have been used for the Schottky diode tests of chapter 9. These five substrates are the culmination of all the research and have used all of the processes, described previously, which have been developed and optimised to give good quality diodes.

The five substrates have been cut from the same wafer which has the following properties;

- Material: Si <100>
- Resistivity: 1-20 ohm/cm
- Doping: p-type (Boron)
- Size: 4” x 525µm thick +/- 25µm
- Description: Single side polished

The wafer is cut into approximately 25mm x 25mm squares using a diamond tipped scribe.

The substrates have been numbered SD2, SD3, SD4, SD6 and SD7.

The substrates have been fabricated to have 8 solid diodes of 1mm diameter and 8 pillar diodes, made up of 400 pillars with a diameter of 50µm each.

A layer of Al has been deposited on the bottom of the wafer to form the ohmic contact once annealed, the thickness of Al is approximately 100nm.

8.12.1 **Photoresist**

The quality of the photoresist determines the quality of the features that will be produced. Some images of the photoresist have been taken for SD2, SD3 and SD4, but no images were taken of the photoresist for SD6 and SD7. However, the profile measurements which have been taken for all five substrates, as shown below, will give an indication of the photoresist quality.

Figure 8-22 below shows the typical photoresist for a SD2 pillar diode, and Figure 8-23 below shows the typical photoresist for a SD2 solid diode.

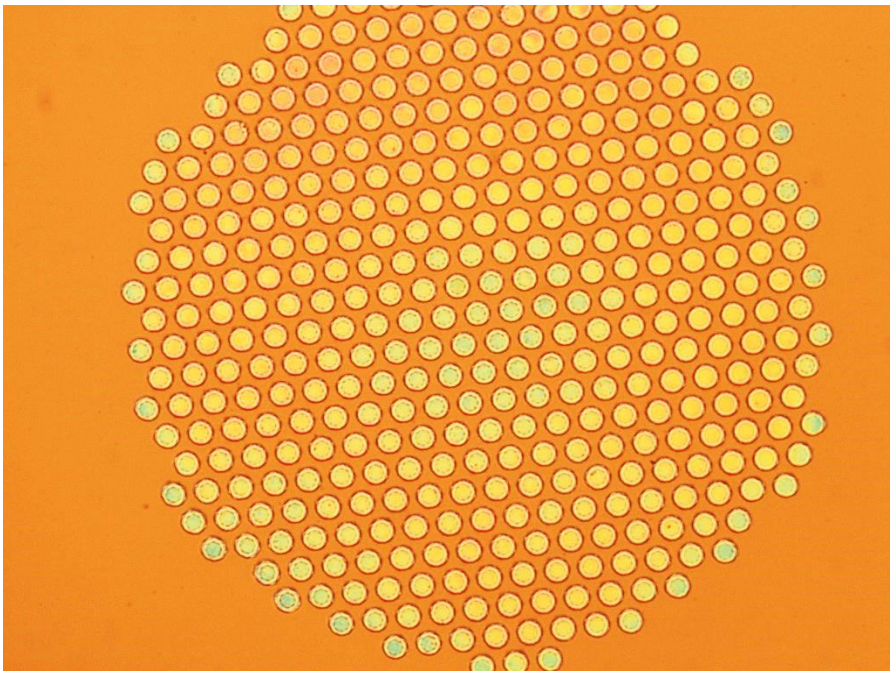

Figure 8-22 - SD2 Typical pillar photoresist optical image

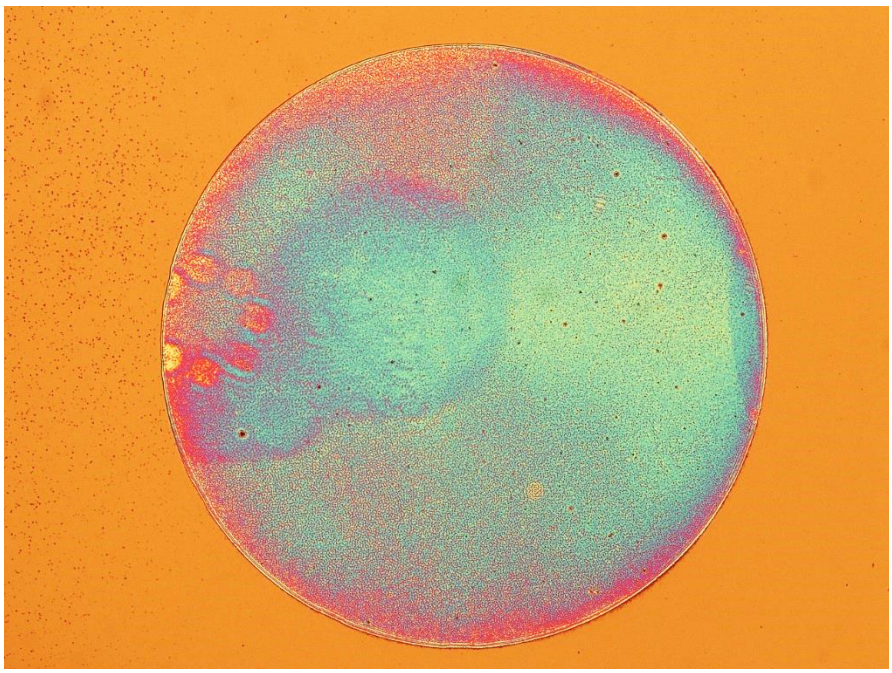

Figure 8-23 - SD2 Typical solid photoresist optical image

With the aid of a programme called ImageJ, it is possible to measure features on an image file, once the image has been calibrated. This is carried out by calibrating between the centre of two pillars, where the length should be 55µm. Using this the pillars in Figure 8-22 above have a diameter of approximately 36µm, and the solid in Figure 8-23 above has a diameter of approximately 985µm. These are both smaller than intended (50µm & 1000µm respectively) and this is most likely due to the sample being over developed.

Figure 8-24 below shows the typical photoresist for a SD3 pillar diode, and Figure 8-25 below shows the typical photoresist for a SD3 solid diode.

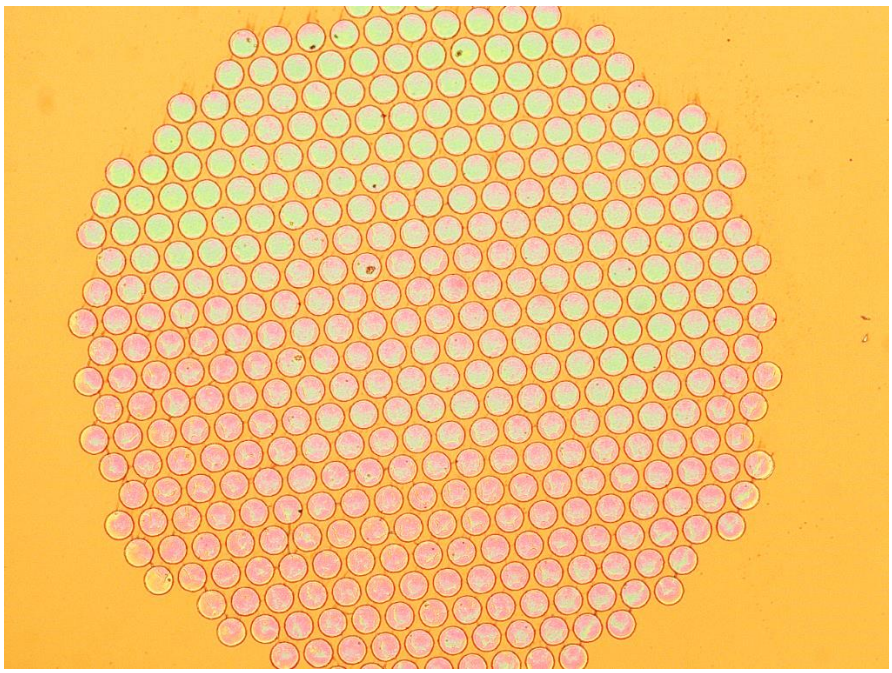

Figure 8-24 - SD3 Typical pillar photoresist optical image

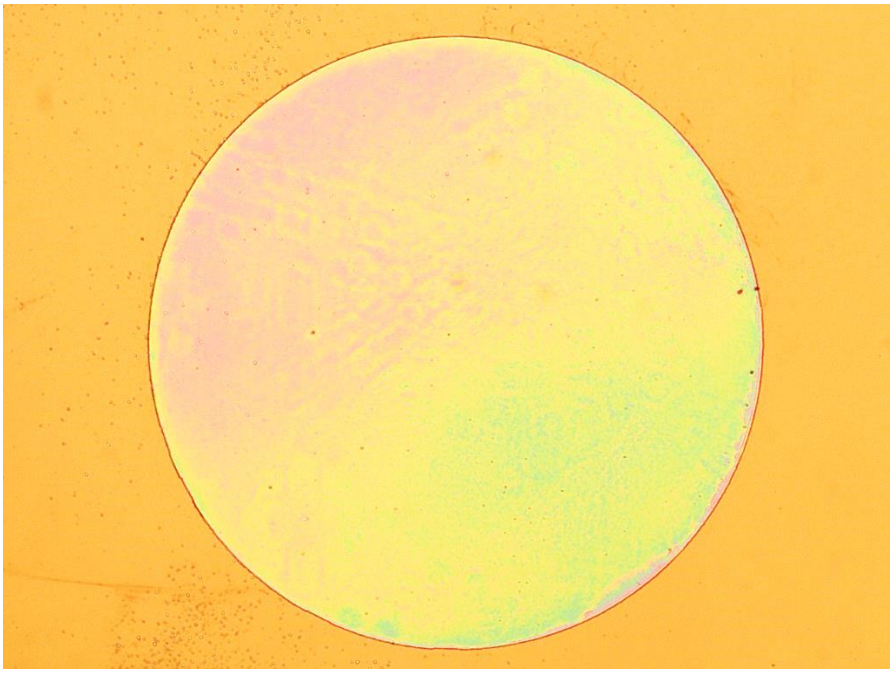

Figure 8-25 - SD3 Typical solid photoresist optical image

Using ImageJ, the pillars in Figure 8-24 above have a diameter of approximately 46µm, and the solid in Figure 8-25 above has a diameter of approximately 996µm. These are very close to the intended sizes (50µm & 1000µm respectively) with just a slight over development.

Figure 8-26 below shows the typical photoresist for a SD4 pillar diode, and Figure 8-27 below shows the typical photoresist for a SD4 solid diode.

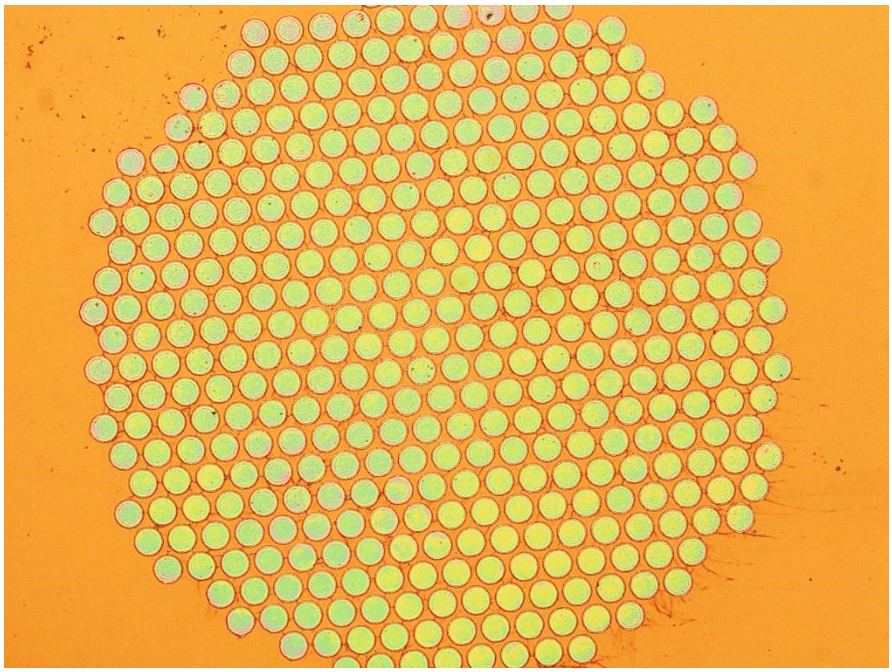

Figure 8-26 - SD4 Typical pillar photoresist optical image

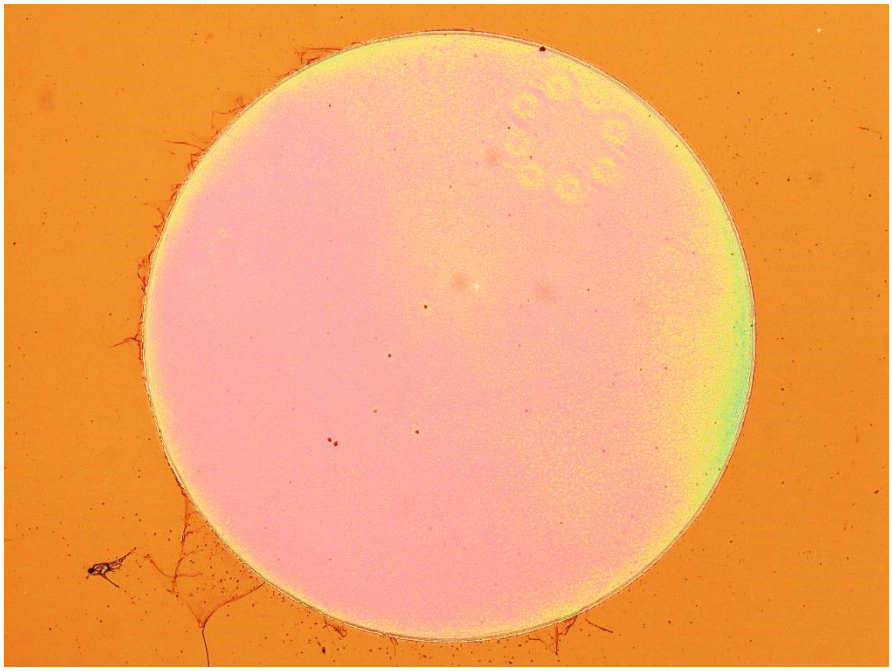

Figure 8-27 - SD4 Typical solid photoresist optical image

Using ImageJ, the pillars in Figure 8-26 above have a diameter of approximately 43µm, and the solid in Figure 8-27 above has a diameter of approximately

993µm. These are close to the intended sizes (50µm & 1000µm respectively) with just a small over development.

A summary of the photoresist measurements is shown in Table 8-6 below.

Substrate	Pillar Diameter (µm)	Solid Diameter (µm)
SD2	36	985
SD3	46	996
SD4	43	993

Table 8-6 - Photoresist measurements summary for SD2, 3 & 4

As seen above, the photoresist has been over developed slightly, and the pillars and solids are smaller than intended. This will affect the Biot number and transient temperature response. With reference to chapter 2 the Biot numbers and transient response time to achieve 50°C temperature change for the designed diameters (50µm and 1000µm) and actual diameters from Table 8-6 above, are shown in Table 8-7 below.

Substrate	Biot Number		Transient response for 50°C temperature change (s)	
	Pillar	Solid	Pillar	Solid
Designed	4.087E-7	5.007E-7	7.851	9.619
SD2	3.801E-7	5.007E-7	7.301	9.618
SD3	4.019E-7	5.007E-7	7.611	9.619
SD4	3.962E-7	5.007E-7	7.611	9.619

Table 8-7 - Biot number and transient response designed against actual

As can be seen from Table 8-7 above, the Biot numbers for the pillars reduce as the diameters reduce and the transient response is quicker for the reduced diameter pillars. These very small changes will not have any significant effect on the transient temperature readings.

8.12.2 **Profiles**

The profiles of all five substrates (SD2, SD3, SD4, SD6, and SD7) have been measured on the Profilometer, set to a distance of 2000µm, and a step of 1µm.

These measurements have been used to mainly measure the etch depth obtained, but can also be used to measure the diameter of the pillars and solids. These measurements have been carried out after the Al has been deposited (500nm). It should be noted that the alignment of the profilometer is manual, and it may be that the stylus is not traversing the maximum diameter of the features, which will lead to an underestimation of the measurements. The measurements and the graphs are presented as indicative only for the diameters, and no conclusions can be derived from the diameter measurements. The average height (etch depth) measurements are presented in chapter 7 and reproduced here in Table 8-8 below for information.

Substrate	Average Etch Depth (µm)
SD2	3.45
SD3	3.27
SD4	3.40
SD6	3.29
SD7	3.07

Table 8-8 - SD2/3/4/6/7 Average etch depth using a profilometer

Figure 8-28 below shows a typical profile for a SD2 pillar diode, and Figure 8-29 below shows a typical profile for a SD2 solid diode. From Figure 8-28 below it is possible to see the thickness of the deposited Al contact at point A, which is showing approximately 500nm.

From Figure 8-28 below the pillar widths have an average measurement of 37µm, and from Figure 8-29 below the solid has an average width of 986µm.

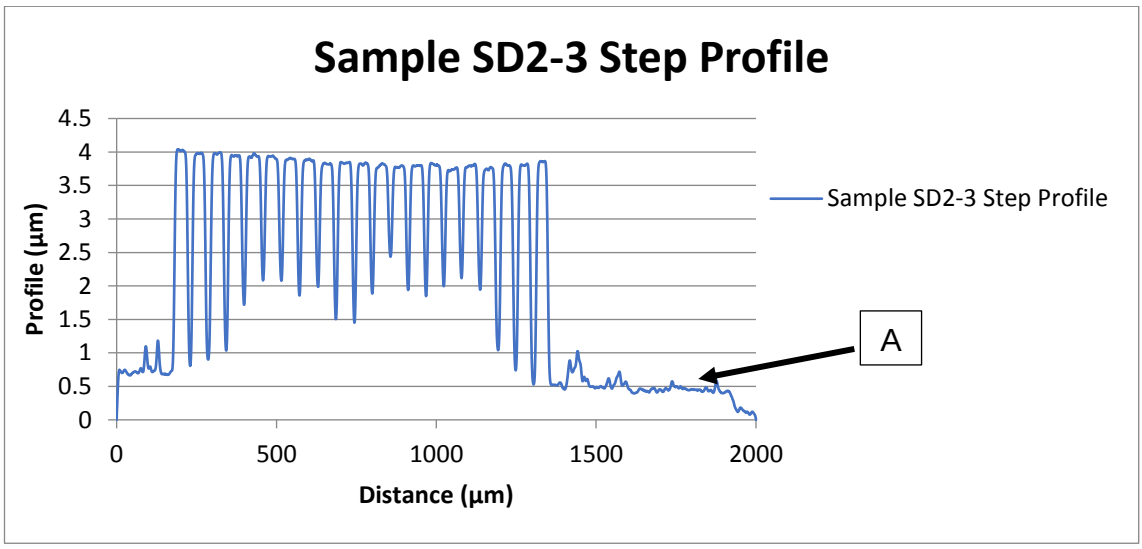

Figure 8-28 - SD2 Typical pillar step profile measured using a profilometer and in addition showing the deposited Al thickness

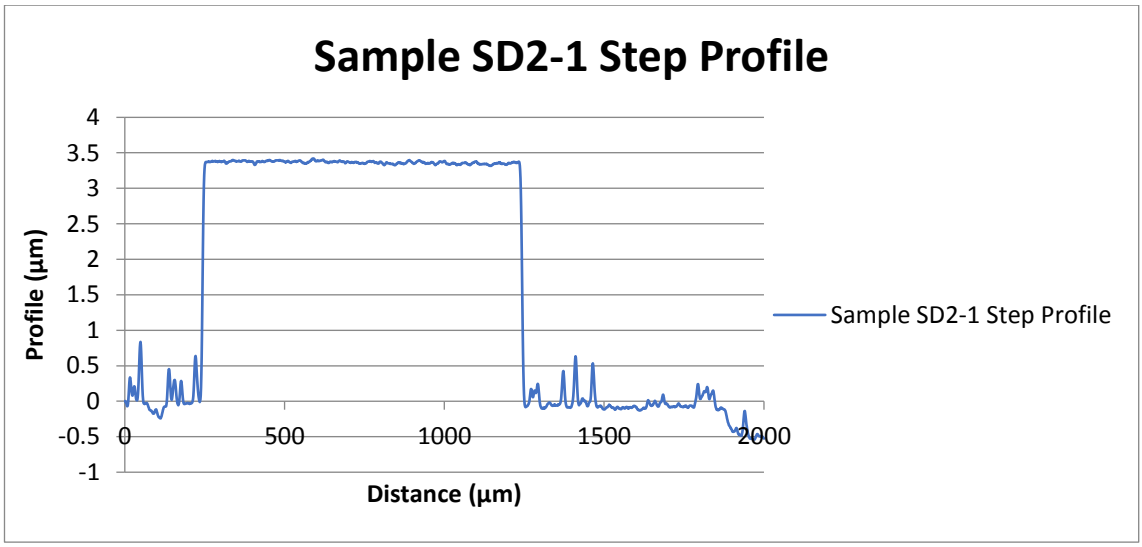

Figure 8-29 - SD2 Typical solid step profile measured with a profilometer

The typical profiles for SD3 are shown in Figure 8-30 for the pillars, and Figure 8-31 for the solid. From Figure 8-30 below the pillar widths have an average measurement of 40µm, and from Figure 8-31 below the solid has an average width of 981µm.

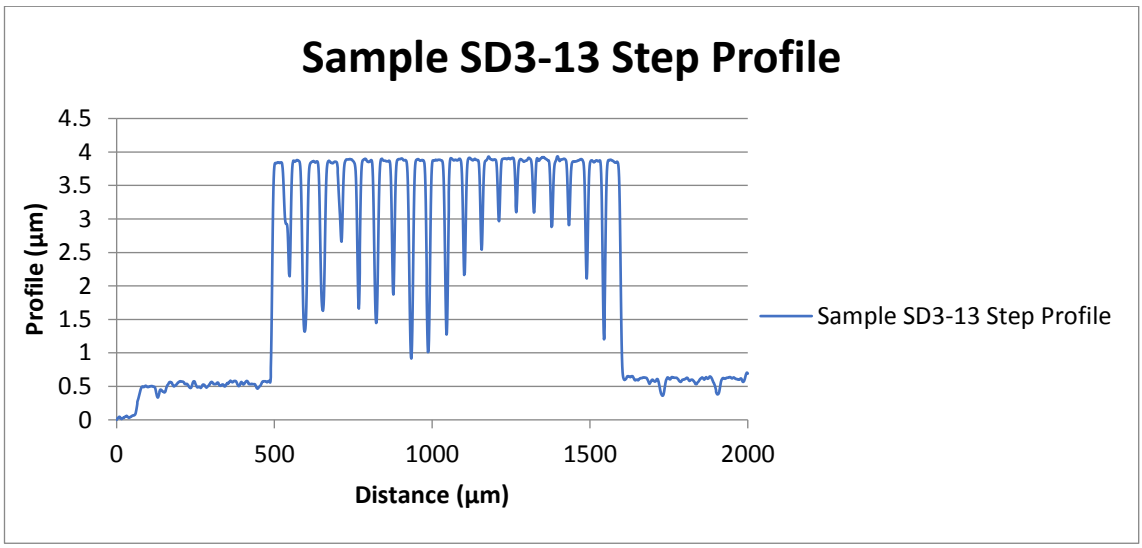

Figure 8-30 - SD3 Typical pillar step profile measured with a Profilometer

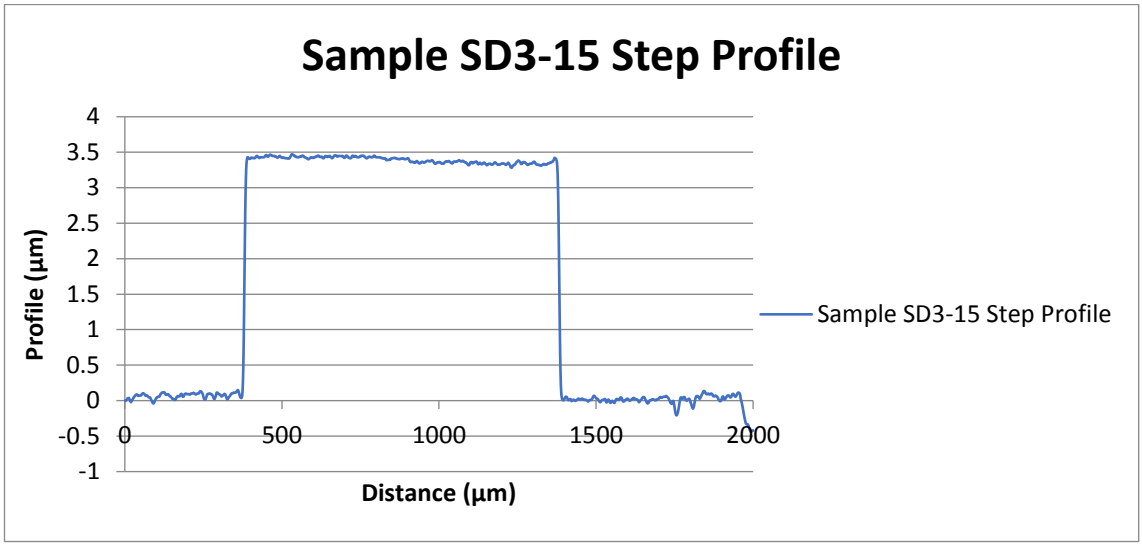

Figure 8-31 - SD3 Typical solid step profile measured with a profilometer

The typical profiles for SD4 are shown in Figure 8-32 for the pillars, and Figure 8-33 for the solid. From Figure 8-32 below the pillar widths have an average measurement of 33µm, and from Figure 8-33 below the solid has an average width of 999µm.

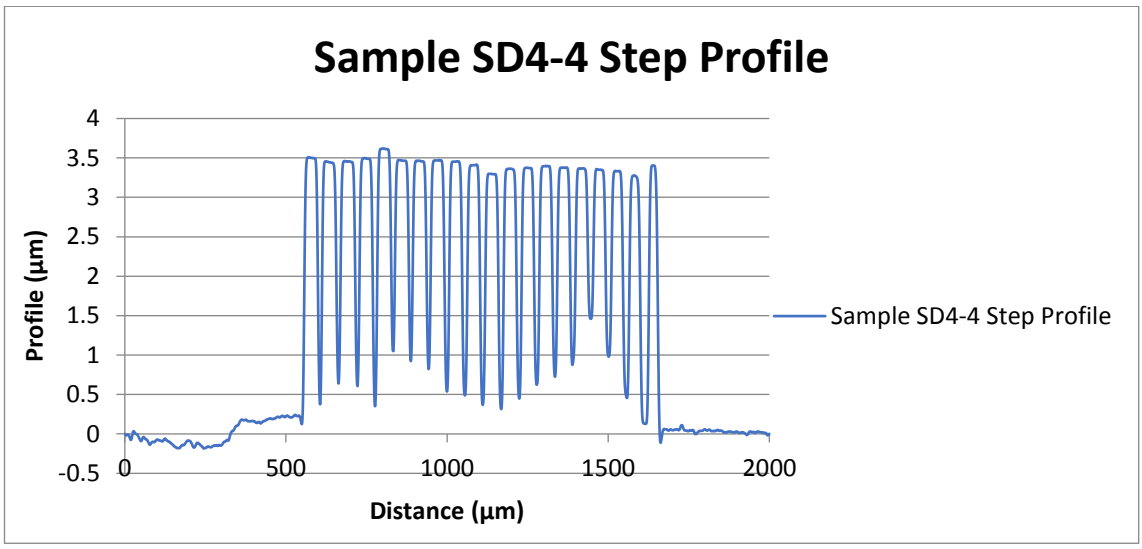

Figure 8-32 - SD4 Typical pillar step profile measured with a Profilometer

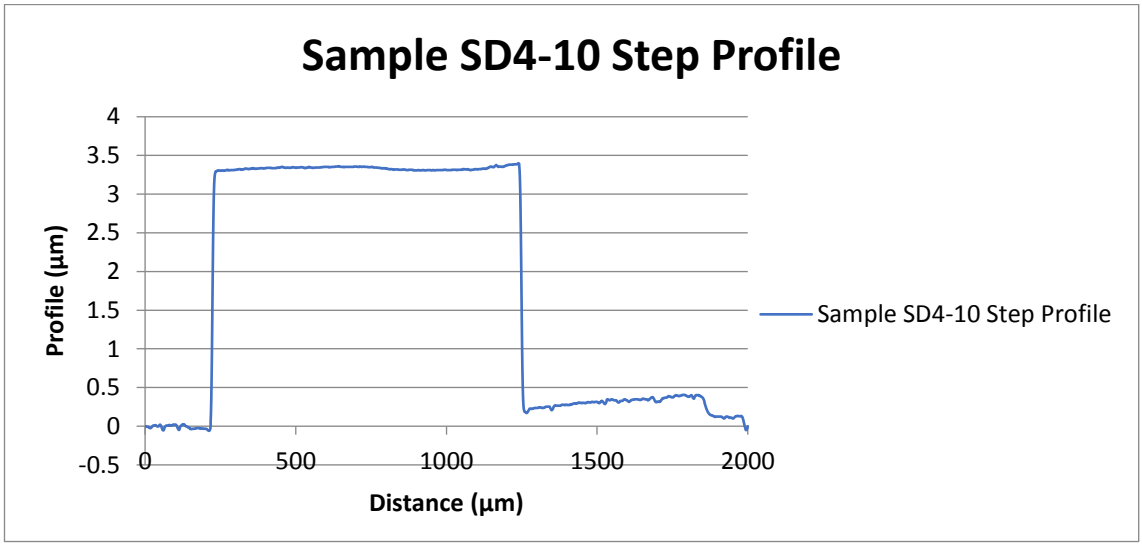

Figure 8-33 - SD4 Typical solid step profile measured with a profilometer

The typical profiles for SD6 are shown in Figure 8-34 for the pillars, and Figure 8-35 for the solid. From Figure 8-34 below the pillar widths have an average measurement of 39µm, and from Figure 8-35 below the solid has an average width of 998µm.

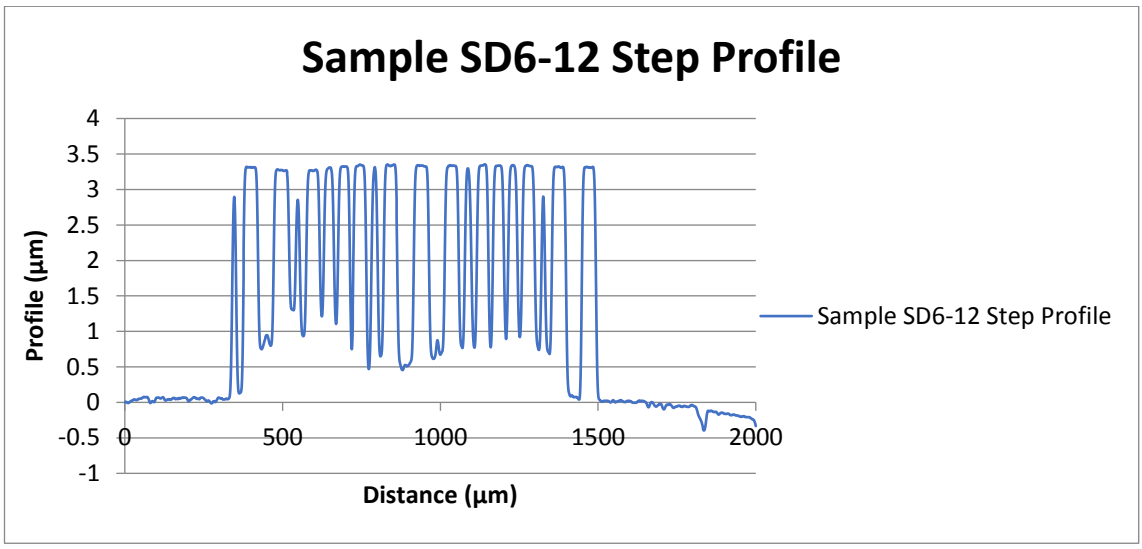

Figure 8-34 - SD6 Typical pillar step profile measured with a Profilometer

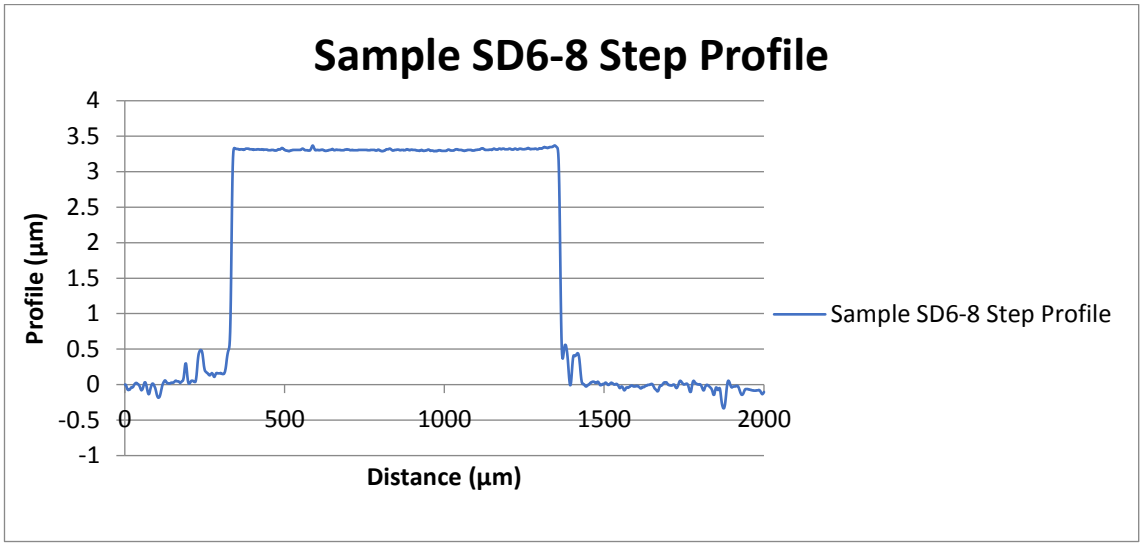

Figure 8-35 - SD6 Typical solid step profile measured with a profilometer

The typical profiles for SD7 are shown in Figure 8-36 for the pillars, and Figure 8-37 for the solid. From Figure 8-36 below the pillar widths have an average measurement of 32µm. As noted above it can be seen that the profilometer does not traverse the centre of the pillars, as they get larger from left to right, and from Figure 8-37 below the solid has an average width of 986µm.

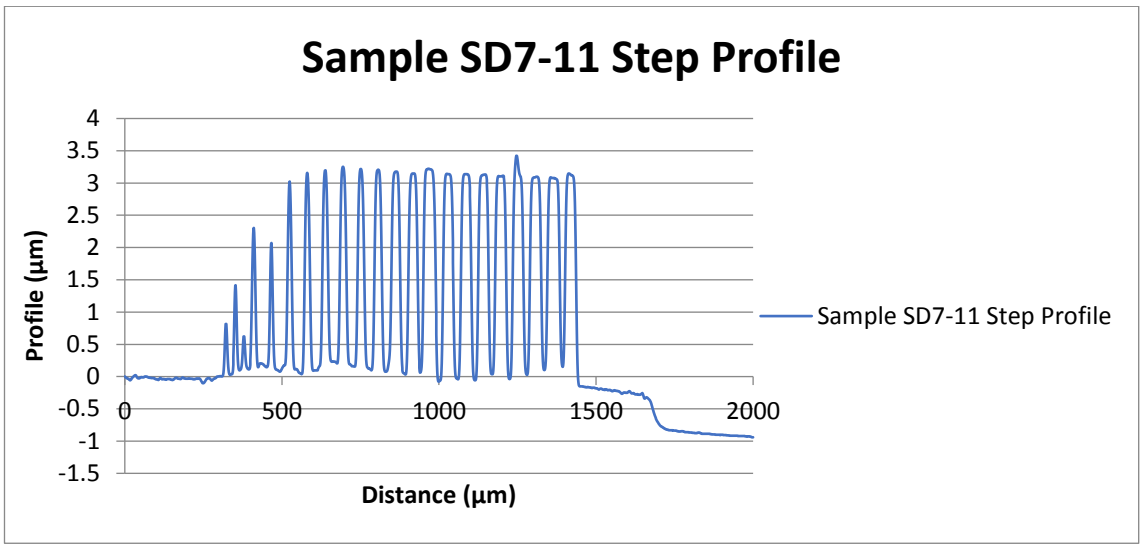

Figure 8-36 - SD7 Typical pillar step profile measured with a Profilometer

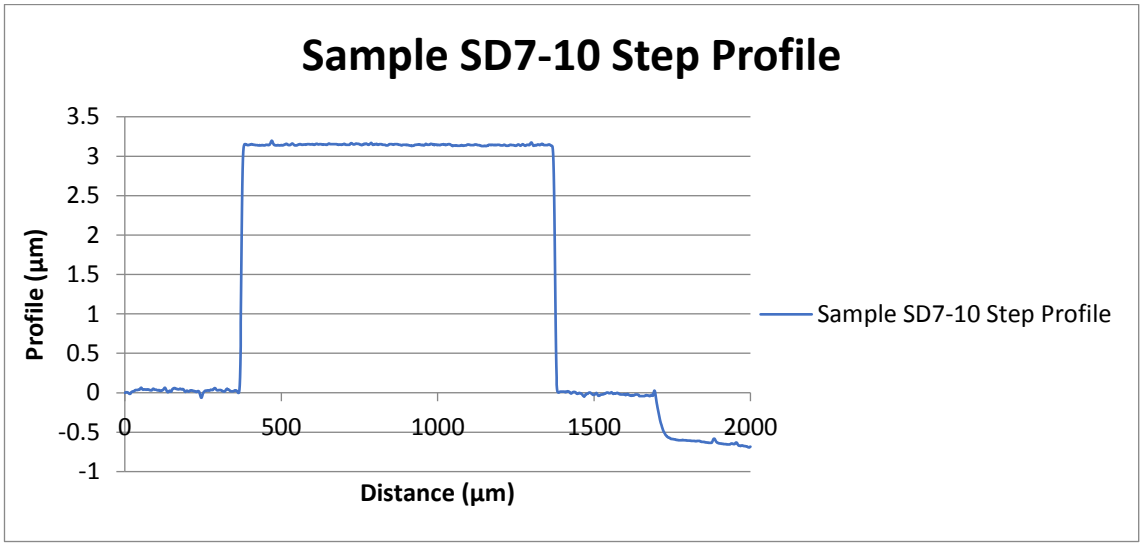

Figure 8-37 - SD7 Typical solid step profile measured with a profilometer

A detailed profile has been obtained for SD3 as shown in Figure 8-38 below, to determine the angle of the etch, which as described in chapter 7 should be 54.7° angle *X* in inset A in Figure 8-38 below will be TAN^{-1} (1.2/0.965) = 51.19° which correlates well very with the theoretical value. The small difference could be due to the Al that has been deposited on the side of the pillar.

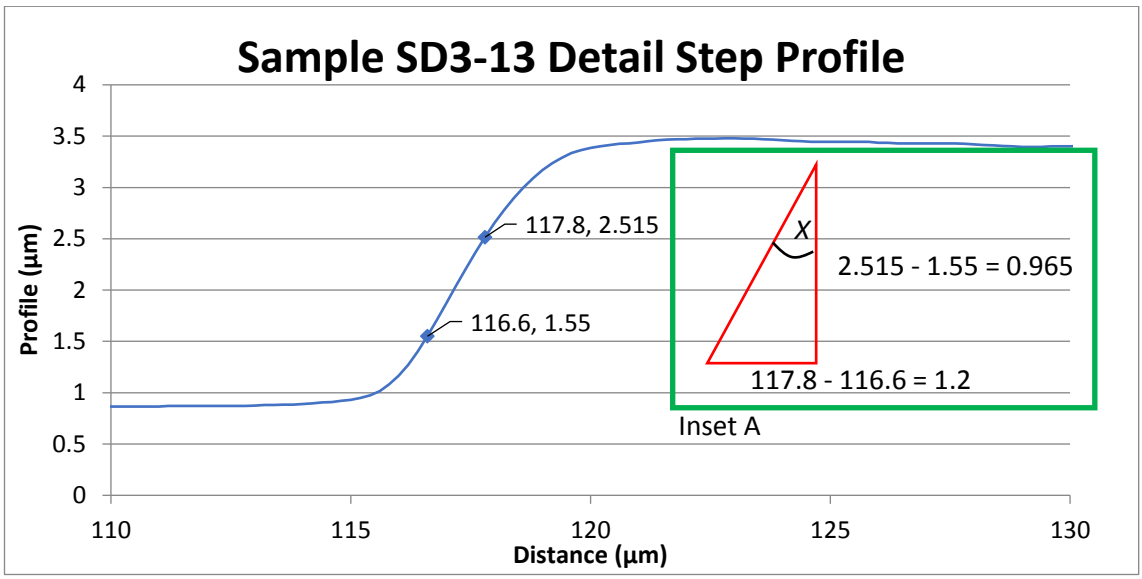

Figure 8-38 - SD3 Detail step profile showing the typical KOH etch angle

From the above details of the five constructed substrates and diodes, it has been shown that they are constructed in such a way, that it should be possible to see a difference in the transient thermal characteristics of the diodes. With the pillar diodes having a greater surface area to volume ratio.

8.13 Solid and Pillar diode SEM Images

Figure 8-39 below is an overall SEM image of SD2-14, and is an SEM image of the produced diodes, and Figure 8-40 is a high magnification image of one of the pillars in SD2-14. This shows the typical KOH etching [104] along the planes of the Si, that produce this octagonal shape (the original Mask was circular). Figure 8-40 also shows the coverage achieved with the top Al contact, the right-hand side seems to have covered the walls of the pillar, but not on the left-hand side. This is due to the orientation of the sample in the evaporator and line of sight.

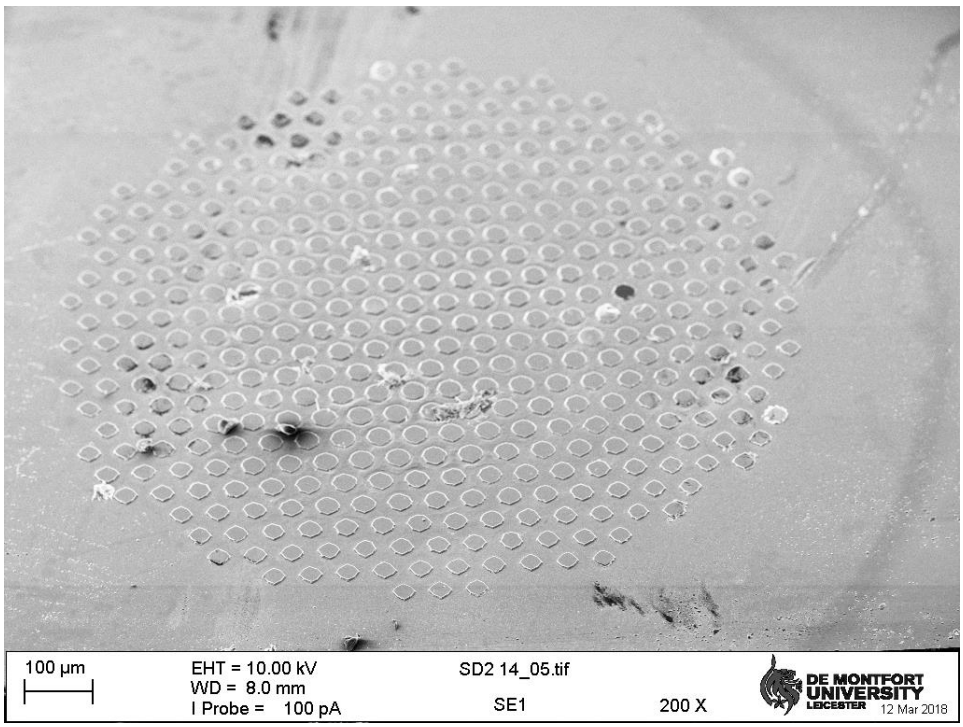

Figure 8-39 - SD2-14 SEM pillar diode image overall

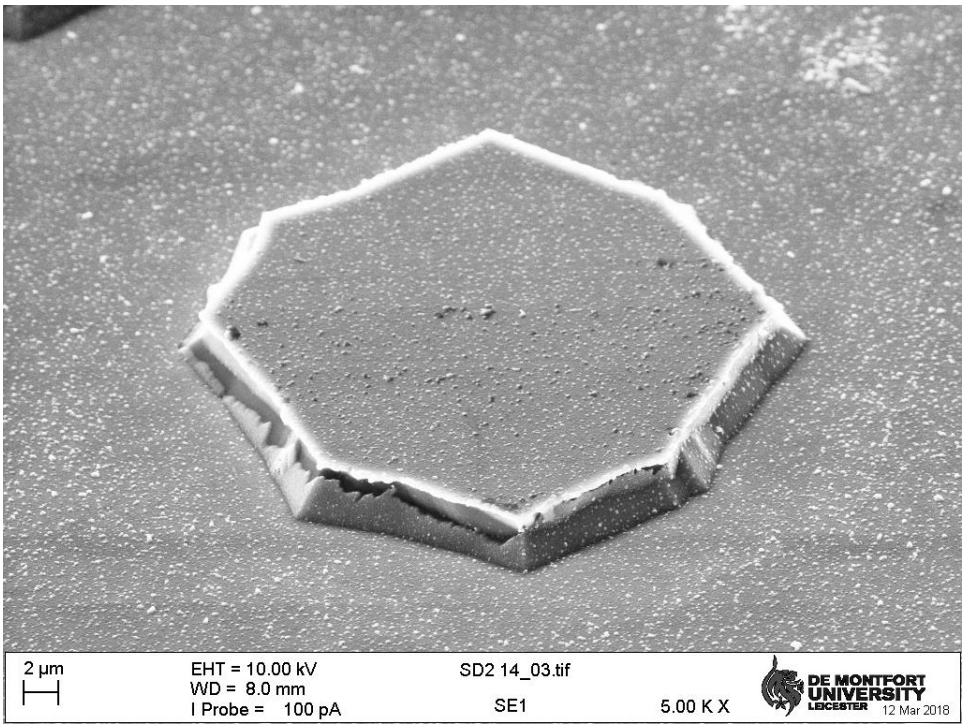

Figure 8-40 - SD2-14 SEM image of a single pillar

Figure 8-41 below shows an overall SEM image of SD2-15, and Figure 8-42 below shows a high magnification of the edge of SD2-15 which shows the Al

coverage on the wall. This also shows typical KOH etching characteristic along the planes.

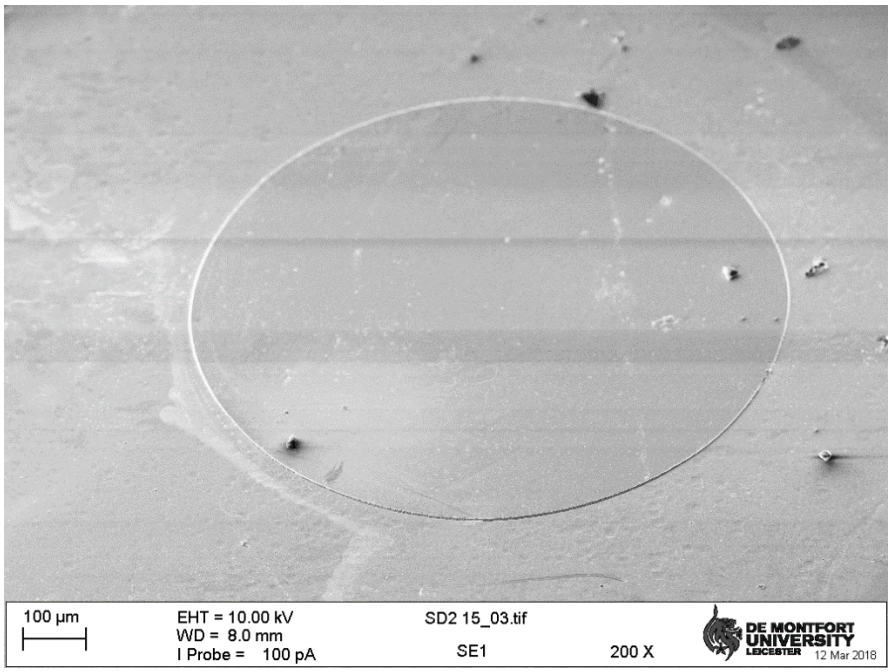

Figure 8-41 - SD2-15 Overall solid diode SEM image

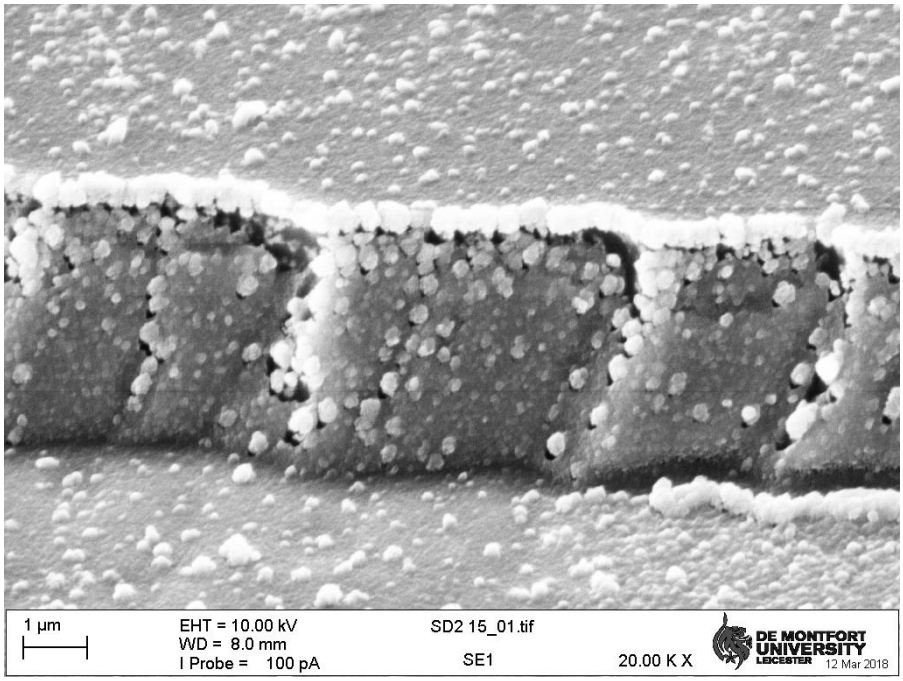

Figure 8-42 - SD-15 High magnification SEM wall image of a solid diode

Chapter 9 **Schottky Diode Testing**

This section describes how the Schottky diodes have been tested to obtain the electrical and temperature characteristics.

9.1 **Introduction**

This will first look at the electrical characteristics of the diodes as listed below.

- Forward biased turn on voltage
- Rectification ratio
- Ideality factor

And secondly look at the temperature measurements achieved, the temperature measurements being the more important ones, to determine the energy efficiency in the pillar diode construction compared to the solid constructed ones.

The testing has been carried out on five substrates, which have been produced from the same wafer and gone through the same concurrent manufacturing processes. Each substrate contains 16 Schottky diodes, 8 made from a solid construction and 8 from a pillar construction, and arranged and numbered on the substrate as shown in Figure 9-1 below.

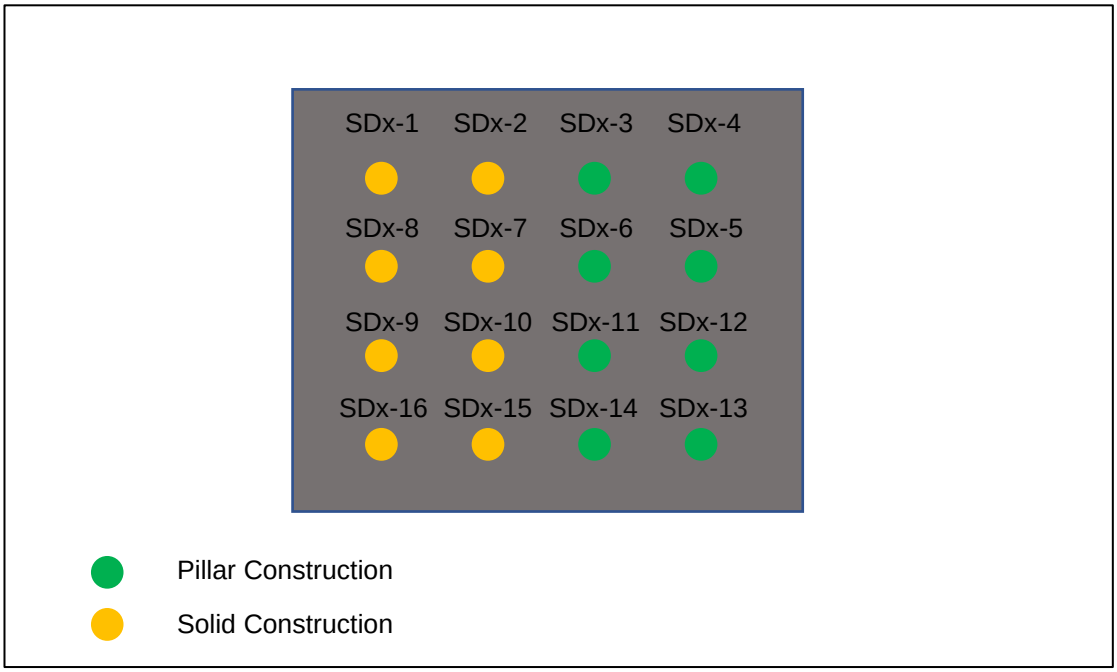

Figure 9-1 - Pillar and solid diode arrangement on substrate

From Figure 9-1 above the “x” is the Schottky diode substrate number, all the substrates that have been used are numbered 2,3,4,6 & 7, and hence, the diode naming convention used shall be for example SD2-3, i.e. substrate 2 and diode 3 which is a diode of pillar construction. As identified in Figure 9-1 above, the yellow dots are the solid constructed diodes, and the green dots are the pillar constructed diodes. This colour convention will be used throughout this chapter.

9.2 Forward Biased turn on voltage

As detailed in section 3.2 the forward biased turn on voltage should be between 0.15V and 0.45V for a Si Schottky diode. This is obtained from the I-V curve, and shall be read as the value when the I-V curve deviates from the horizontal zero line, as indicated in Figure 9-2 below. The turn on voltage for this device is 0.22V. All I-V measurements have been taken between -1 V and +1 V.

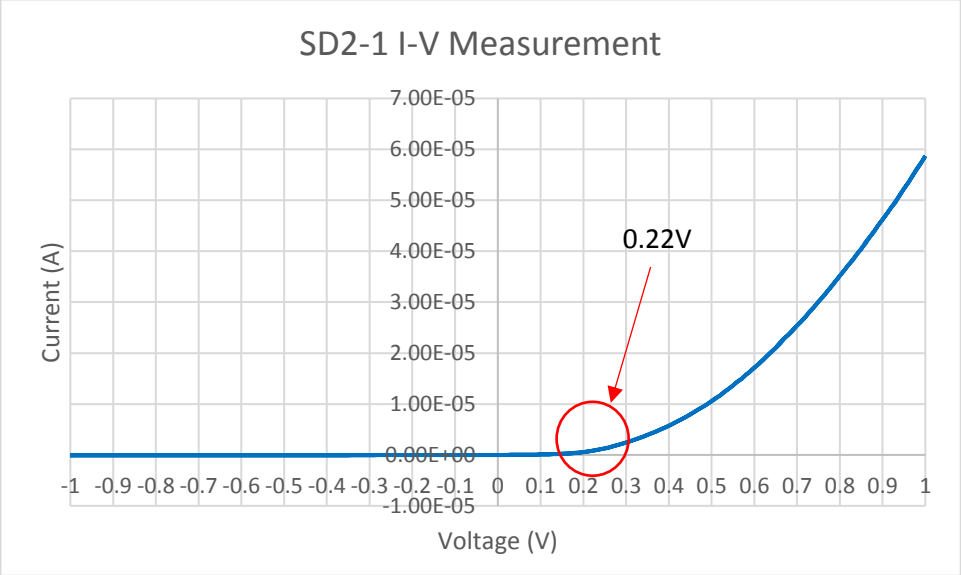

Figure 9-2 - SD2-1 I-V Measurement showing the turn on voltage point

The tables below detail the turn on voltages for the five substrates.

SD2 - Turn on Voltage															
Diode Number															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0.22	0.23	0.17	0.13	0.17	0.18	0.2	0.22	0.21	0.24	0.2	0.1	0.15	0.14	0.2	0.12

Table 9-1 - SD2 Forward biased turn on voltages

SD3 - Turn on Voltage															
Diode Number															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0.2	0.23	0.22	0.21	0.27	0.16	0.17	0.37	0.37	0.16	0.17	0.12	0.09	0.07	0.21	0.37

Table 9-2 - SD3 Forward biased turn on voltages

SD4 - Turn on Voltage															
Diode Number															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0.18	0.2	0.17	0.2	0.21	0.19	0.21	0.2	0.2	0.2	0.17	0.11	0.19	0.19	0.19	0.2

Table 9-3 - SD4 Forward biased turn on voltages

SD6 - Turn on Voltage															
Diode Number															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0.26	0.26	0.12	0.25	0.11	0.14	0.24	0.31	0.27	0.26	0.25	0.24	0.22	0.2	0.18	0.22

Table 9-4 - SD6 Forward biased turn on voltages

SD7 - Turn on Voltage															
Diode Number															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0.18	0.17	0.14	U/S	0.17	0.16	0.16	0.18	0.18	0.15	0.15	0.16	0.16	0.16	0.16	0.18

Table 9-5 - SD7 Forward biased turn on voltages

The majority of the forward biased turn on voltages are within the expected range, and there are none above the expected range, but there are a few which are below the expected range of 0.15V. There are obvious issues with the manufacture of these diodes, but this should not have an effect on the temperature measurements. Diode SD7-4 does not give a rectifying behaviour and is behaving like just an ohmic contact and will not be used.

Table 9-6 below summaries the turn on voltage ranges obtained for each of the substrates.

Turn on Voltage Summary		
Substrate	Low (V)	High (V)
SD2	0.10	0.24
SD3	0.07	0.37
SD4	0.11	0.21
SD6	0.11	0.27
SD7	0.14	0.18

Table 9-6 - SD2/3/4/6/7 Forward biased turn on voltage summary

9.3 Rectification ratio

As discussed in section 3.3, the rectification ratio is a comparison between the forward and reversed biased conditions, and gives an indication of how good the Schottky diode is, with an order of greater than two required for the currents on a semi Log scale. For comparison of the Schottky diodes manufactured, the forward and reverse currents at -1V and +1V will be used to provide the rectification ratio, the tables below show the rectification ratios obtained for the five substrates.

SD2 - Rectification Ratio												
Diode No.	1			2			3			4		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-1.11E-07	5.87E-05	2.72	-1.31E-08	4.62E-05	3.55	-6.8E-07	3.7E-05	1.73	-1.5E-06	3.8E-05	1.39
Diode No.	5			6			7			8		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-5.7E-07	2.1E-05	1.56	-7.5E-07	2.2E-05	1.46	-9.3E-09	2.2E-05	3.37	-4.7E-09	2.2E-05	3.67
Diode No.	9			10			11			12		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-7.1E-08	2.2E-05	2.49	-2.6E-08	0.00002	2.89	-3.8E-08	1.6E-05	2.64	-1.1E-06	2.1E-05	1.27
Diode No.	13			14			15			16		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-6.4E-07	1.8E-05	1.44	-2E-07	1.9E-05	1.97	-2.2E-08	1.8E-05	2.92	-4.9E-07	1.9E-05	1.59

Table 9-7 - SD2 Rectification ratios

SD3 - Rectification Ratio												
Diode No.	1			2			3			4		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-5.66E-06	3.30E-04	1.77	-1.63E-08	1.84E-05	3.05	-7.37E-08	2.26E-05	2.49	-1.38E-09	3.79E-04	5.44
Diode No.	5			6			7			8		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-2.74E-07	6.48E-05	2.37	-4.59E-07	2.19E-05	1.68	-2.41E-07	2.22E-05	1.96	-8.66E-08	4.34E-04	3.70
Diode No.	9			10			11			12		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-1.38E-09	3.79E-04	5.44	-1.17E-06	1.58E-05	1.13	-7.05E-06	1.54E-05	0.34	-1.54E-06	7.95E-05	1.71
Diode No.	13			14			15			16		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-1.04E-05	8.94E-05	0.93	-3.99E-06	7.42E-06	0.27	-1.97E-08	4.34E-06	2.34	-8.28E-08	3.53E-04	3.63

Table 9-8 - SD3 Rectification ratios

SD4 - Rectification Ratio												
Diode No.	1			2			3			4		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-2.56E-08	1.84E-05	2.86	-1.40E-09	1.63E-05	4.07	-9.72E-08	1.44E-05	2.17	-5.08E-09	1.36E-05	3.43
Diode No.	5			6			7			8		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-1.09E-08	1.21E-05	3.05	-3.03E-08	1.36E-05	2.65	-1.24E-09	1.31E-05	4.02	-3.66E-09	1.42E-05	3.59
Diode No.	9			10			11			12		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-2.42E-09	1.44E-05	3.77	-2.09E-09	1.47E-05	3.85	-9.89E-08	1.41E-05	2.15	-5.69E-07	1.35E-05	1.38
Diode No.	13			14			15			16		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-3.41E-08	1.08E-05	2.50	-4.55E-08	1.41E-05	2.49	-3.47E-09	1.46E-05	3.62	-2.12E-09	1.46E-05	3.84

Table 9-9 - SD4 Rectification ratios

SD6 - Rectification Ratio												
Diode No.	1			2			3			4		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-1.96E-09	6.40E-05	4.51	-1.70E-09	5.38E-05	4.50	-6.23E-06	7.26E-05	1.07	-4.51E-09	6.07E-05	4.13
Diode No.	5			6			7			8		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-2.72E-06	6.51E-05	1.38	-9.17E-07	6.57E-05	1.86	-2.32E-09	6.31E-05	4.43	-3.50E-09	4.96E-05	4.15
Diode No.	9			10			11			12		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-1.45E-09	5.53E-05	4.58	-1.72E-09	5.55E-05	4.51	-7.90E-09	5.59E-05	3.85	-2.11E-08	5.73E-05	3.43
Diode No.	13			14			15			16		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-2.91E-08	5.76E-05	3.30	-2.79E-07	6.01E-05	2.33	-3.44E-06	5.97E-05	1.24	-9.64E-09	5.13E-05	3.73

Table 9-10 - SD6 Rectification ratios

SD7 - Rectification Ratio												
Diode No.	1			2			3			4		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-2.71E-09	2.35E-05	3.94	-3.14E-09	2.18E-05	3.84	-3.55E-07	2.13E-05	1.78	-1.37E-05	2.33E-05	0.23
Diode No.	5			6			7			8		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-6.47E-09	2.10E-05	3.51	-8.50E-09	2.05E-05	3.38	-5.08E-09	1.80E-05	3.55	-3.04E-09	1.87E-05	3.79
Diode No.	9			10			11			12		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-3.62E-09	1.95E-05	3.73	-5.35E-09	2.00E-05	3.57	-1.57E-08	2.03E-05	3.11	-5.98E-09	2.05E-05	3.54
Diode No.	13			14			15			16		
	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio	Current (A) @		Ratio
	-1V	+1v		-1V	+1v		-1V	+1v		-1V	+1v	
	-5.25E-09	2.05E-05	3.59	1.03E-08	2.10E-05	3.31	-7.36E-09	2.06E-05	3.45	-3.99E-09	1.78E-05	3.65

Figure 9-3 - SD7 Rectification ratios

The rectification ratio on almost all the diodes is above the two order that is required, some a lot better than others, Table 9-11 below summarises the ranges of rectification ratio for the five substrates.

Substrate	Low	High
SD2	1.27	3.67
SD3	0.34	5.44
SD4	1.38	4.07
SD6	1.07	4.58
SD7	0.23	3.94

Table 9-11 - SD2/3/4/6 & 7 Summary of rectification ratios

9.4 **Ideality Factor**

As discussed in section 3.4, the ideality factor shows how good the diode is in the forward biased mode of operation, and is a measure of how fast the forward biased current increases, with a change in forward voltage. The ideal diode would have a factor of 1. The tables below show the ideality factors which have been obtained from the manufactured diodes.

SD2 Ideality Factors									
1					2				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	4.62E-05	5.87E-05	**16.14**	0.90	1.00	3.65E-05	4.62E-05	**16.40**
3					4				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	2.91E-05	3.67E-05	**16.66**	0.90	1.00	2.99E-05	3.75E-05	**17.06**
5					6				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.65E-05	2.08E-05	**16.69**	0.90	1.00	1.73E-05	2.19E-05	**16.39**
7					8				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.70E-05	2.18E-05	**15.54**	0.90	1.00	1.70E-05	2.19E-05	**15.26**
9					10				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.70E-05	2.17E-05	**15.83**	0.90	1.00	1.56E-05	2.00E-05	**15.55**
11					12				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.28E-05	1.63E-05	**15.99**	0.90	1.00	1.66E-05	2.05E-05	**18.31**
13					14				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.42E-05	1.77E-05	**17.54**	0.90	1.00	1.48E-05	1.85E-05	**17.32**
15					16				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.41E-05	1.80E-05	**15.83**	0.90	1.00	1.49E-05	1.89E-05	**16.25**

Table 9-12 - SD2 Ideality factors

SD3 Ideality Factors									
1					2				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	2.83E-04	3.33E-04	**23.75**	0.90	1.00	1.49E-05	1.84E-05	**18.32**
3					4				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.86E-05	2.26E-05	**19.84**	0.90	1.00	3.08E-04	3.79E-04	**18.63**
5					6				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	5.37E-05	6.48E-05	**20.57**	0.90	1.00	1.50E-05	2.19E-05	**10.21**
7					8				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.59E-05	2.22E-05	**11.58**	0.90	1.00	3.56E-04	4.34E-04	**19.51**
9					10				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	3.08E-04	3.79E-04	**18.63**	0.90	1.00	1.18E-05	1.58E-05	**13.24**
11					12				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.13E-05	1.54E-05	**12.48**	0.90	1.00	6.84E-05	7.95E-05	**25.70**
13					14				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	7.65E-05	8.94E-05	**24.80**	0.90	1.00	6.11E-06	7.42E-06	**19.90**
15					16				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	3.35E-06	4.34E-06	**14.93**	0.90	1.00	2.90E-04	3.53E-04	**19.66**

Table 9-13 - SD3 Ideality factors

SD4 Ideality Factors									
1					2				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.51E-05	1.84E-05	**19.55**	0.90	1.00	1.34E-05	1.63E-05	**19.73**
3					4				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.19E-05	1.44E-05	**20.27**	0.90	1.00	1.13E-05	1.36E-05	**20.86**
5					6				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.00E-05	1.21E-05	**20.27**	0.90	1.00	1.11E-05	1.36E-05	**19.03**
7					8				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.07E-05	1.31E-05	**19.10**	0.90	1.00	1.17E-05	1.42E-05	**19.96**
9					10				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.16E-05	1.44E-05	**17.87**	0.90	1.00	1.20E-05	1.47E-05	**19.04**
11					12				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.17E-05	1.41E-05	**20.71**	0.90	1.00	1.15E-05	1.35E-05	**24.10**
13					14				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	9.31E-06	1.08E-05	**26.03**	0.90	1.00	1.17E-05	1.41E-05	**20.71**
15					16				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.22E-05	1.46E-05	**21.52**	0.90	1.00	1.19E-05	1.46E-05	**18.90**

Table 9-14 - SD4 Ideality factors

SD6 Ideality Factors									
1					2				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.40	0.50	8.11E-06	1.74E-05	**5.06**	0.50	0.60	8.71E-06	1.78E-05	**5.41**
3					4				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.30	0.40	1.68E-05	2.76E-05	**7.78**	0.40	0.50	1.02E-05	1.99E-05	**5.78**
5					6				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.30	0.40	1.15E-05	2.02E-05	**6.86**	0.30	0.40	1.17E-05	2.13E-05	**6.45**
7					8				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.40	0.50	9.94E-06	2.11E-05	**5.13**	0.60	0.70	1.48E-05	2.47E-05	**7.55**
9					10				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.50	0.60	1.34E-05	2.38E-05	**6.73**	0.50	0.60	1.48E-05	2.51E-05	**7.32**
11					12				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.40	0.50	9.05E-06	1.78E-05	**5.71**	0.40	0.50	1.20E-05	2.13E-05	**6.74**
13					14				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.40	0.50	1.22E-05	2.15E-05	**6.82**	0.40	0.50	1.41E-05	2.35E-05	**7.57**
15					16				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.40	0.50	1.18E-05	2.12E-05	**6.60**	0.50	0.60	1.49E-05	2.29E-05	**8.99**

Table 9-15 - SD6 Ideality factors

SD7 Ideality Factors									
1					2				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.81E-05	2.35E-05	**14.80**	0.90	1.00	1.70E-05	2.18E-05	**15.54**
3					4				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.66E-05	2.13E-05	**15.50**	0.90	1.00	1.88E-05	2.33E-05	**18.01**
5					6				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.61E-05	2.10E-05	**14.55**	0.90	1.00	1.62E-05	2.05E-05	**16.42**
7					8				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.43E-05	1.80E-05	**16.79**	0.90	1.00	1.47E-05	1.87E-05	**16.06**
9					10				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.54E-05	1.95E-05	**16.37**	0.90	1.00	1.57E-05	2.00E-05	**15.97**
11					12				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.58E-05	2.03E-05	**15.42**	0.90	1.00	1.60E-05	2.05E-05	**15.59**
13					14				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.59E-05	2.05E-05	**15.21**	0.90	1.00	1.60E-05	2.10E-05	**14.21**
15					16				
V1	V2	J1	J2	**η**	V1	V2	J1	J2	**η**
0.90	1.00	1.61E-05	2.06E-05	**15.68**	0.90	1.00	1.39E-05	1.78E-05	**15.63**

Table 9-16 - SD7 Ideality factors

As can be seen from the tables above the ideality factor is not close to 1, which suggests that there is some internal series resistance in the manufactured diodes, which is limiting the rate of increase of the diode current. Although not ideal this should not affect the temperature measurements.

Summarised below in Table 9-17 are the ideality factor ranges for the five substrates.

Substrate	Low	High
SD2	15.26	18.31
SD3	10.21	25.70
SD4	17.87	26.03
SD6	5.06	8.99
SD7	14.21	18.01

Table 9-17 - SD2/3/4/6/7 Summary of Ideality factors

The ideality factor ranges, as detailed in Table 9-17, are not ideal but they are not much different to what has been reported before, Park et al [26] reports 7 to 9, Chintakula et al [22] reports 12 to 30 and Guduru et al [34] reports 8.1 to 10. There can be a number of reasons for this, usually due to defects introduced when making the diodes which lead to a high series resistance between the metal contacts and the semiconductor, caused by oxide layers and defects.

9.5 Electrical Characteristic summary

In summary the devices which have the lowest turn on voltage, usually below the normally expected level of 0.15V have a lower rectification ratio and a higher ideality factor.

9.6 Temperature Measurements

Temperature measurements have been carried out to compare the pillar constructed diodes, and the solid constructed diodes, to see if the high volume to surface area ratio of the pillar diodes, would make a difference on the ability to dissipate more heat. The production of heat is a by-product of passing current through a diode, and is wasted energy. Operating the diodes cooler will make them more energy efficient. Chapter 5 discusses the method of temperature

measurement that has been designed, as part of this research, to validate this hypothesis. This method has been used for all temperature measurements.

9.6.1 Whole substrate temperature measurements

The first Schottky diode temperature measurements were taken with all of the 16 diodes, on the one substrate, as manufactured. However, it became clear that the substrate itself was having an impact on the readings obtained, and the readings seemed to be random in nature and no conclusions could be drawn. This has been validated by taking one of the early samples produced (PR73), and taking temperature readings of the 16 diodes, all on the one substrate, then this was cut into strips containing four diodes on each, and finally these strips were cut in half to leave two diodes per substrate, as detailed in Figure 9-4 below.

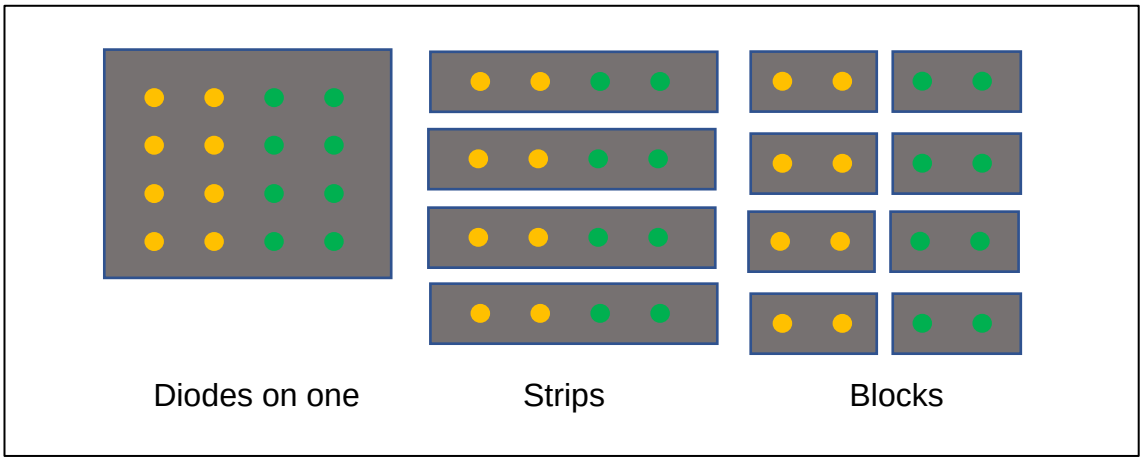

Figure 9-4 - PR73 Substrate cut up into strips and blocks

Temperature measurements were taken for all of the diodes, at each of the three stages. The temperatures and powers for each of the stages were averaged and plotted, average temperature difference vs average power as shown in Figure 9-5 below.

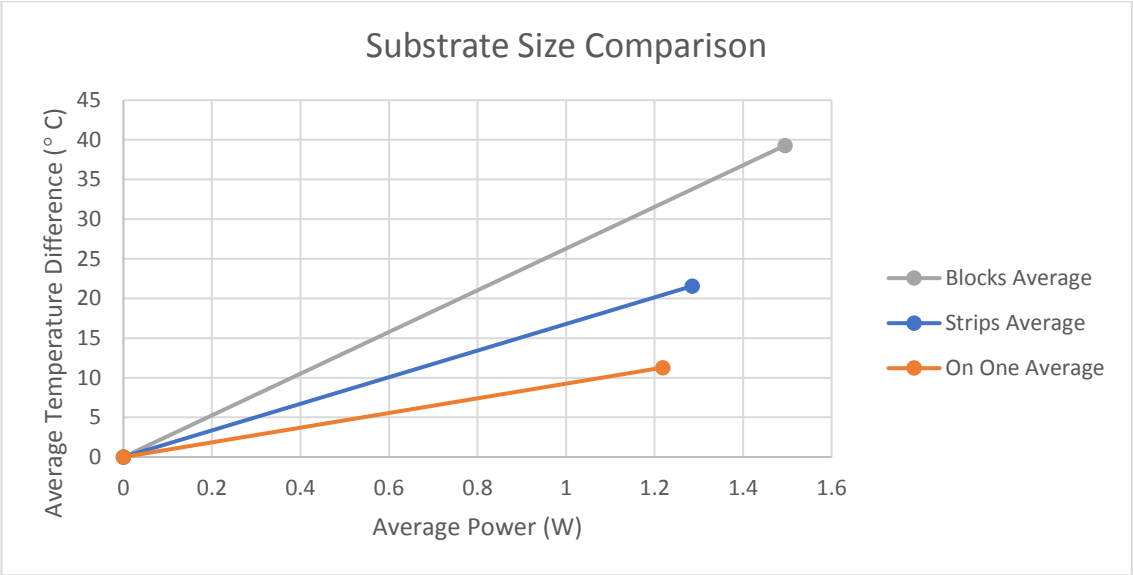

Figure 9-5 - Substrate size comparison with temperature

Figure 9-5 shows that the smaller the size of substrate the larger the temperature difference, indicating that not only the diode is heating up but also the substrate as well, which is leading to the substrate damping the effect of the pillar diodes greater surface area to volume ratio.

In addition, because of the way in which PR73 was cut into blocks, i.e. either 2 solid or 2 pillar diodes per block, it was not possible to carry out any temperature comparisons, due to the difficulty in cutting the substrate up into equal sized blocks, without the diodes being on the same size substrate comparisons cannot be made.

Further diodes have been produced and cut up slightly differently as detailed in the next section.

9.7 Block substrate Temperature Measurements

As mentioned above to get a block that can be used for comparison purposes one of each type of diode needs to be on the block, thus five further substrates (SD 2,3,4,6 &7) have been cut up as detailed below in Figure 9-6.

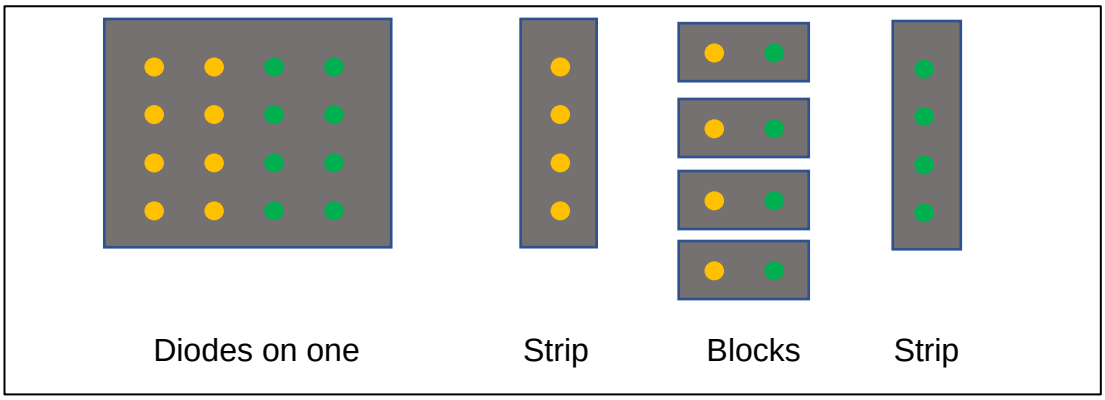

Figure 9-6 - Diagram of how SD2/3/4/6 & 7 substrates have been cut up

It should be noted that the cutting of the substrate is reasonably easy, and the cut generally follows the crystalline structure. However, this is not always the case, and some of the blocks from the five substrates have been destroyed. The blocks that are remaining, and have been tested, are detailed in Table 9-18 below.

	Diode Blocks Remaining			
Substrate	2 & 3	6 & 7	10 & 11	14 & 15
SD2	No	Yes	Yes	No
SD3	Yes	Yes	Yes	Yes
SD4	Yes	Yes	Yes	Yes
SD6	Yes	Yes	Yes	No
SD7	No	No	Yes	Yes

Table 9-18 - SD2/3/4/6/7 Diode blocks remaining after being cut and still usable

Figure 9-7, Figure 9-8, Figure 9-9, Figure 9-10 & Figure 9-11 below show the substrates cut up into blocks, and the bottom contact Al foil attached ready for testing. Highlighted are the diodes, which have been damaged and will not form part of these results. From the figures it can be seen that they are not on the same size substrate, which means no comparison can be made between the different blocks, due to the substrate having an effect on the temperature readings obtained as discussed above.

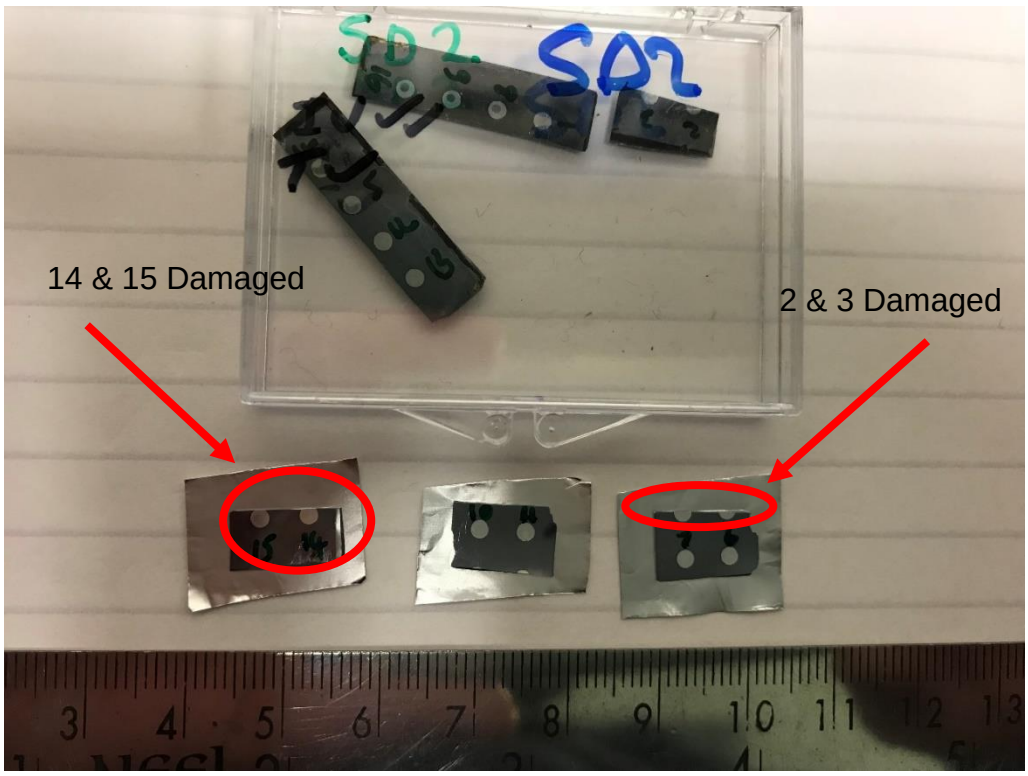

Figure 9-7 - Photo of SD2 substrate cut up showing damaged diodes

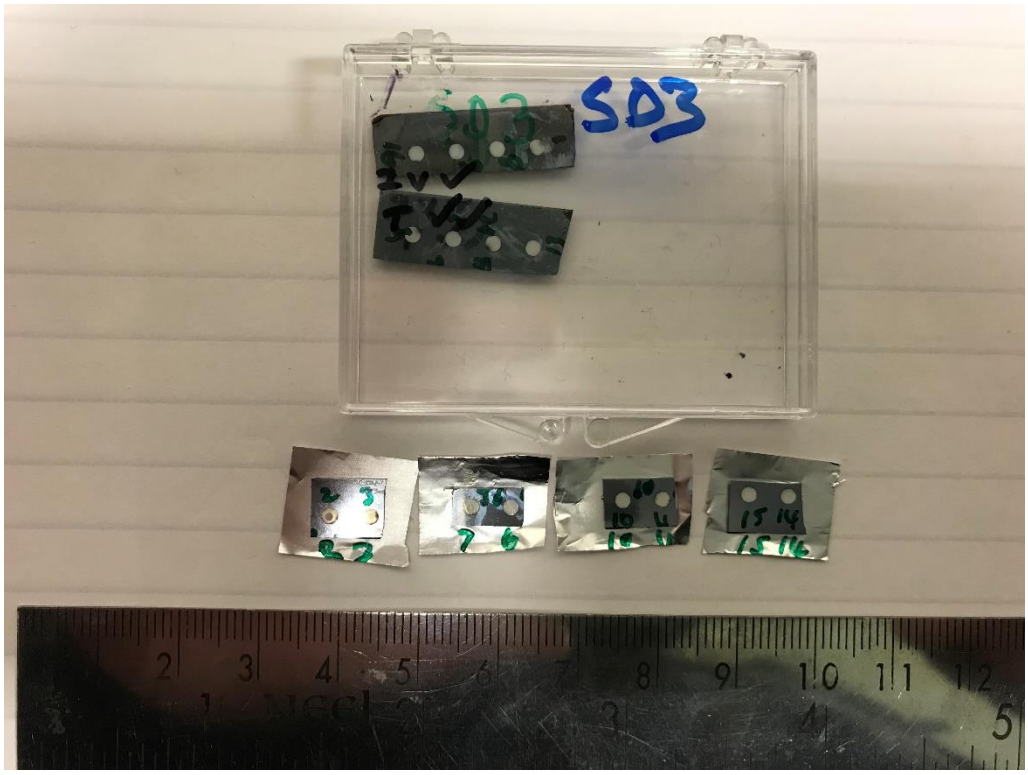

Figure 9-8 - Photo of SD3 substrate cut up

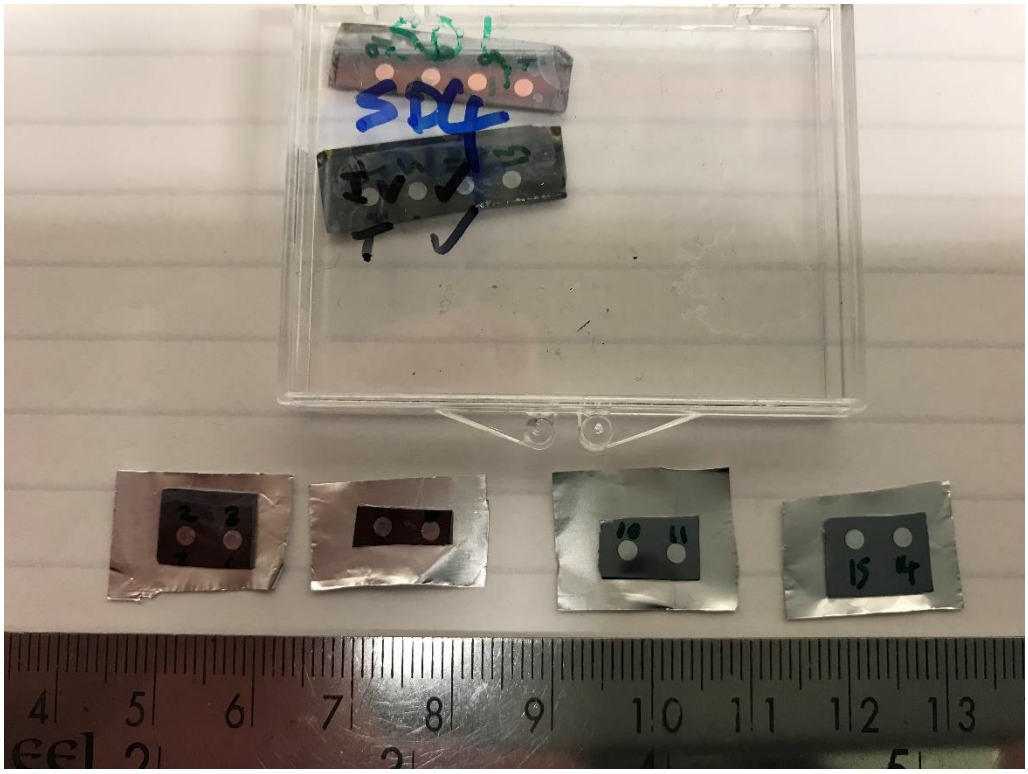

Figure 9-9 - Photo of SD4 substrate cut up

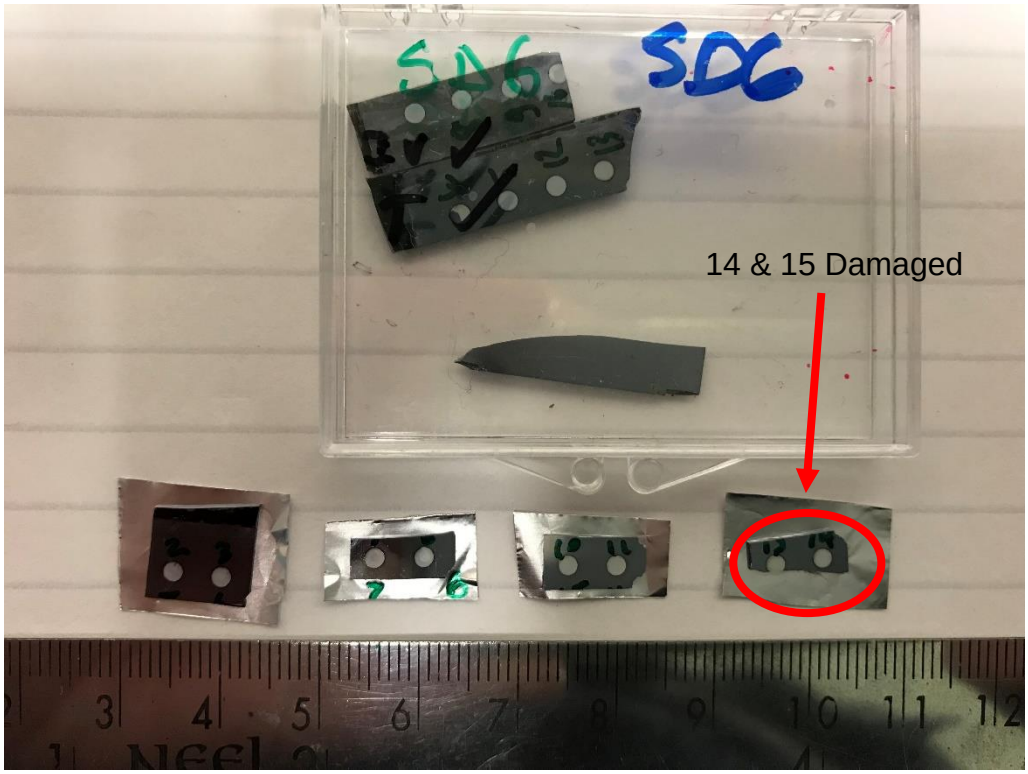

Figure 9-10 - Photo of SD6 substrate cut up showing damaged diodes

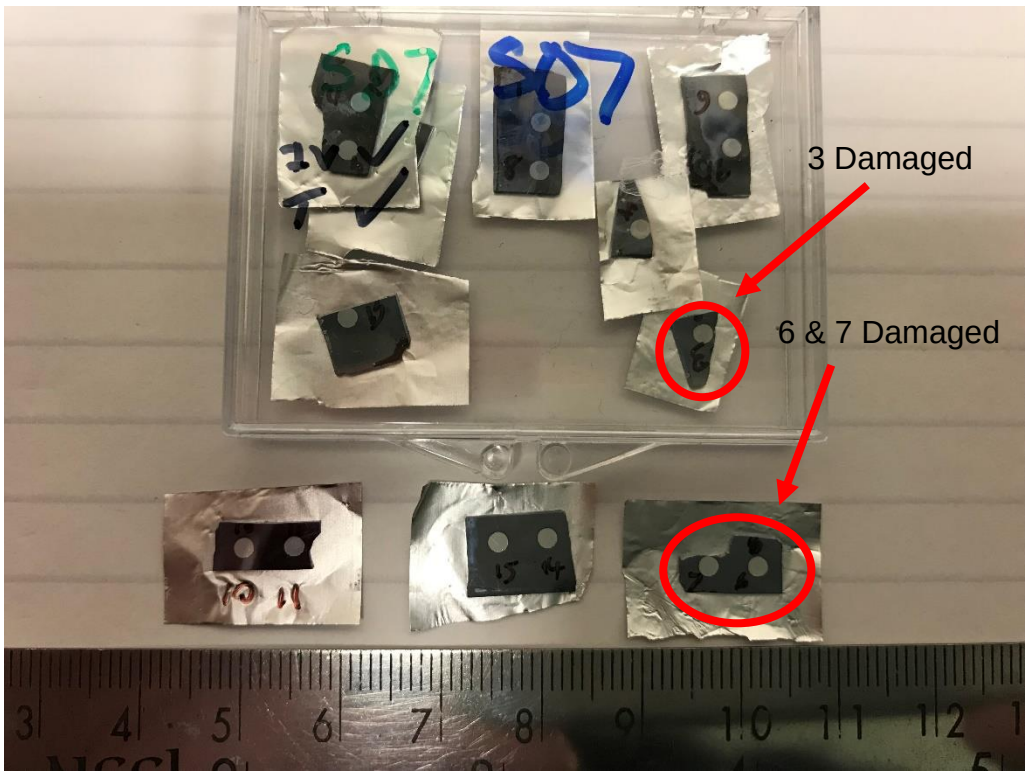

Figure 9-11 - Photo of SD7 substrate cut up showing damaged diodes

As detailed in Chapter 5 rising and falling temperatures are recorded for the Schottky diodes. The following sections show the graphs which have been produced for the five substrates, and each graph contains both the diodes on each of the blocks for comparison purposes. The ones named X-Dot are the diodes made from Pillars, the ones named X-Sol are the solid diodes.

9.7.1 **Substrate SD2**

Below are the temperature graphs obtained for SD2 diodes 6,7,10 & 11.

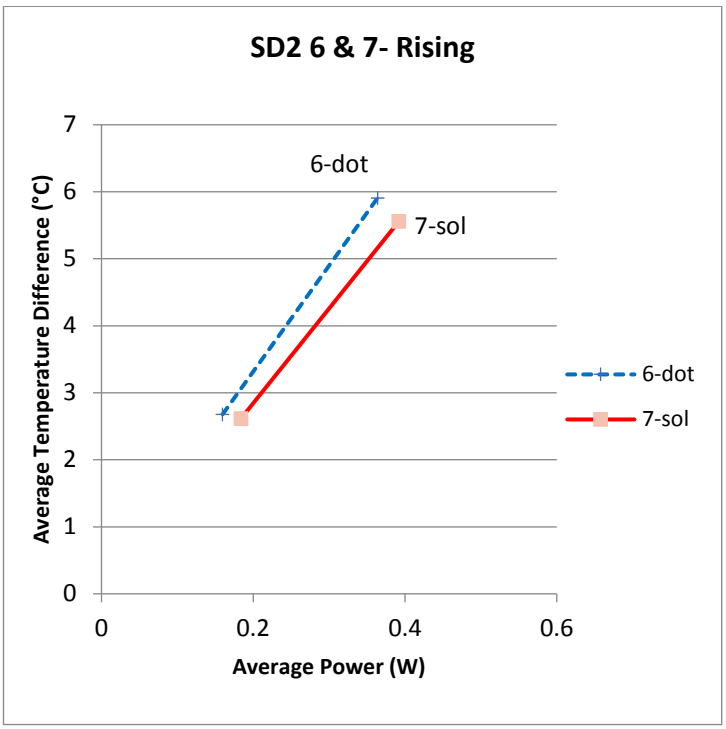

Figure 9-12 - SD2 6 & 7 Rising temperatures graph

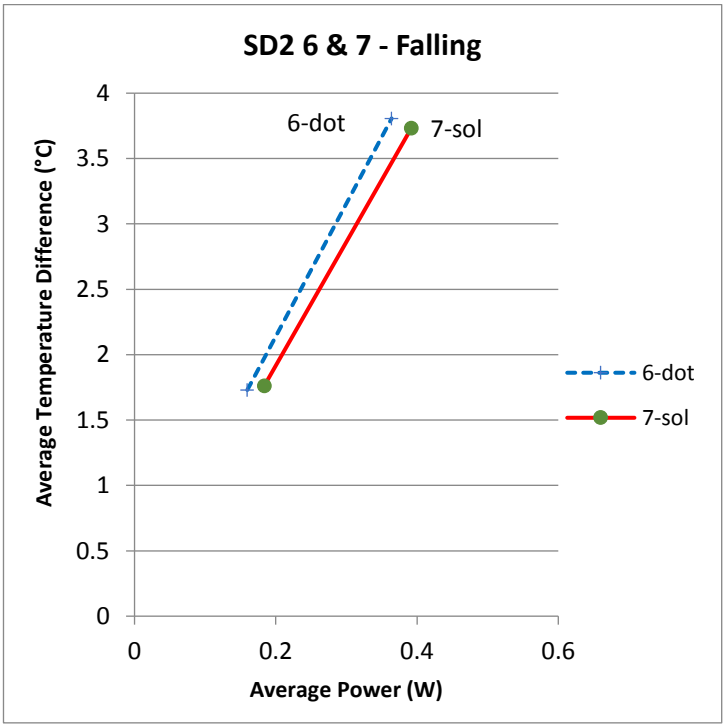

Figure 9-13 - SD2 6 & 7 Falling temperatures graph

Figure 9-14 - SD2 10 & 11 Rising temperatures graph

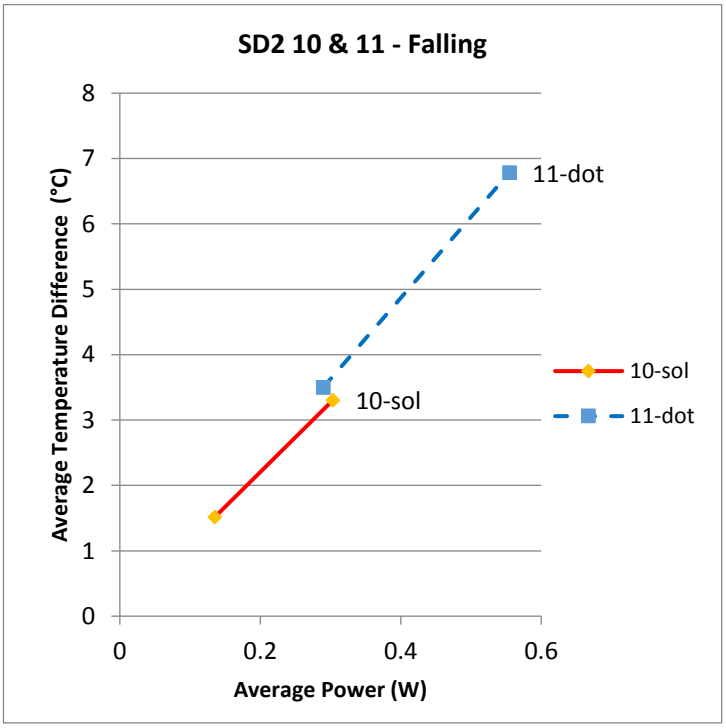

Figure 9-15 - SD2 10 & 11 Falling temperatures graph

9.7.2 **Substrate SD3**

Below are the temperature graphs obtained for SD3 diodes 2,3,6,7,10,11,14 & 15.

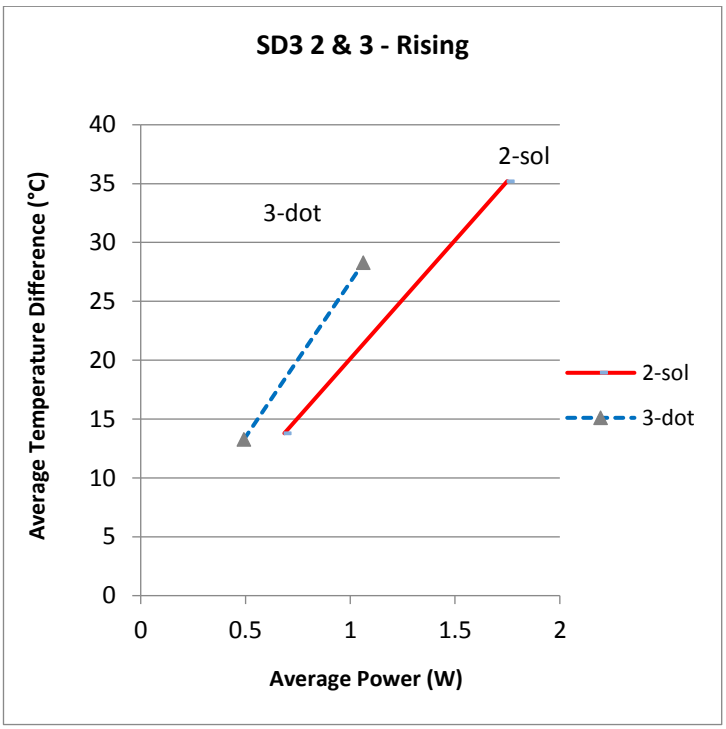

Figure 9-16 - SD3 2 & 3 Rising temperatures graph

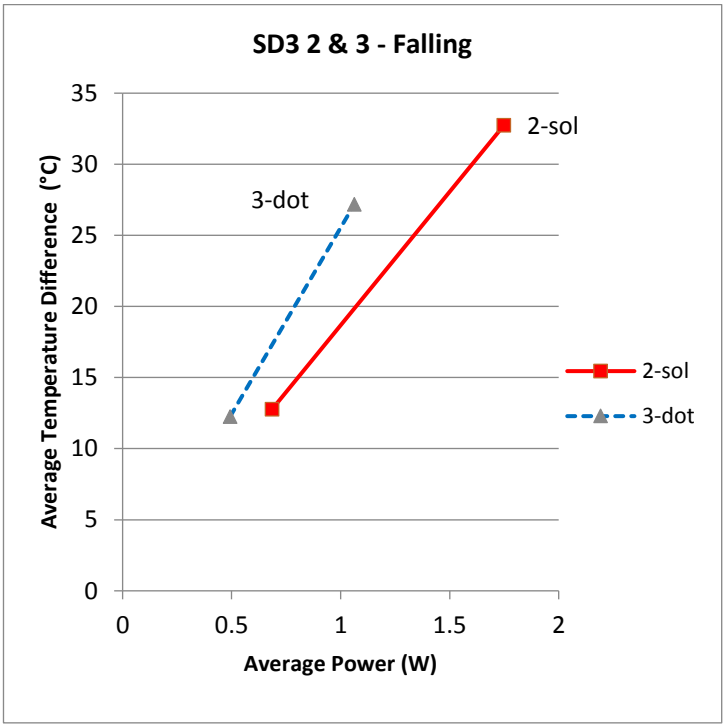

Figure 9-17 - SD3 2 & 3 Falling temperatures graph

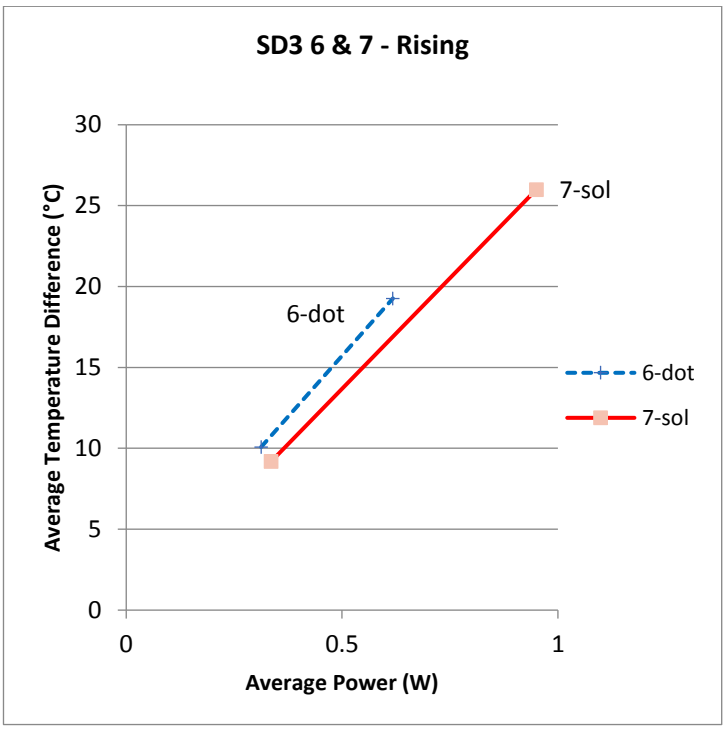

Figure 9-18 - SD3 6 & 7 Rising temperatures graph

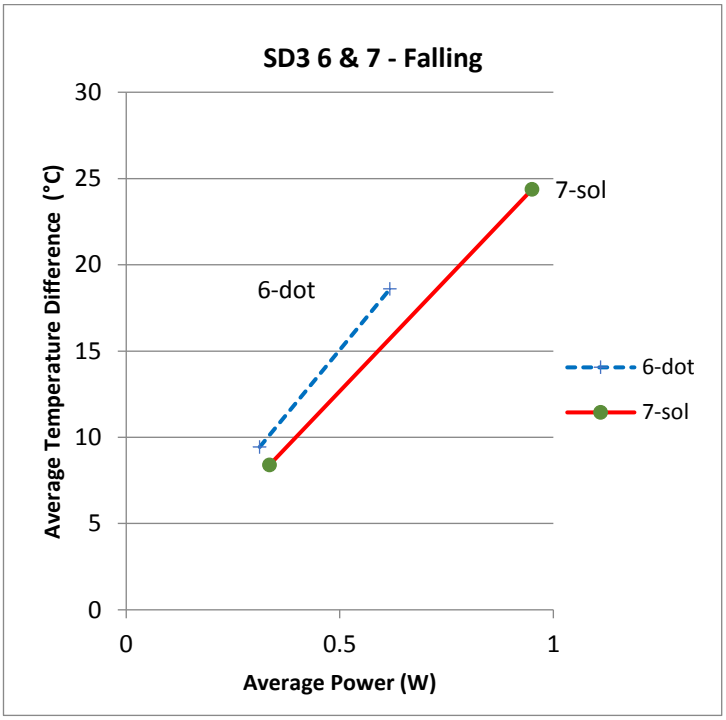

Figure 9-19 - SD3 6 & 7 Falling temperatures graph

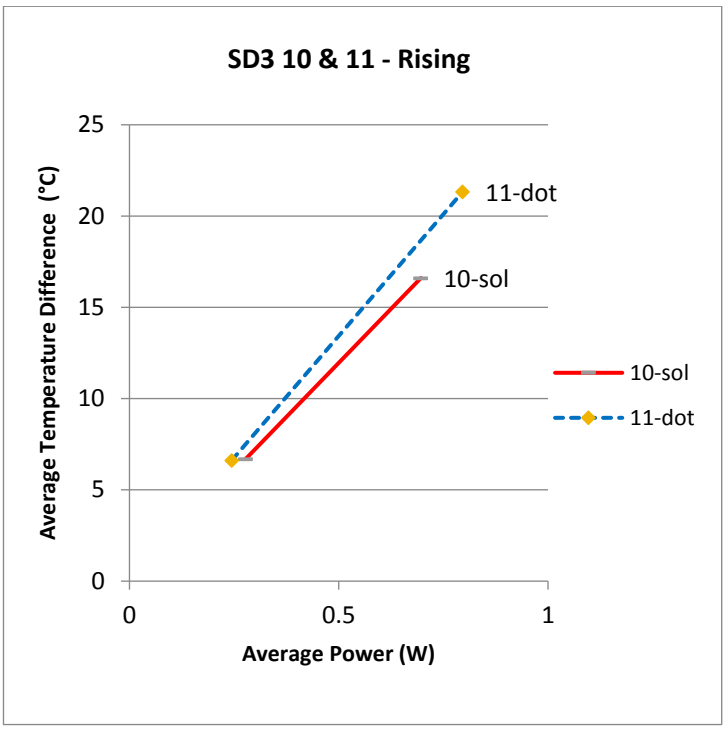

Figure 9-20 - SD3 10 & 11 Rising temperatures graph

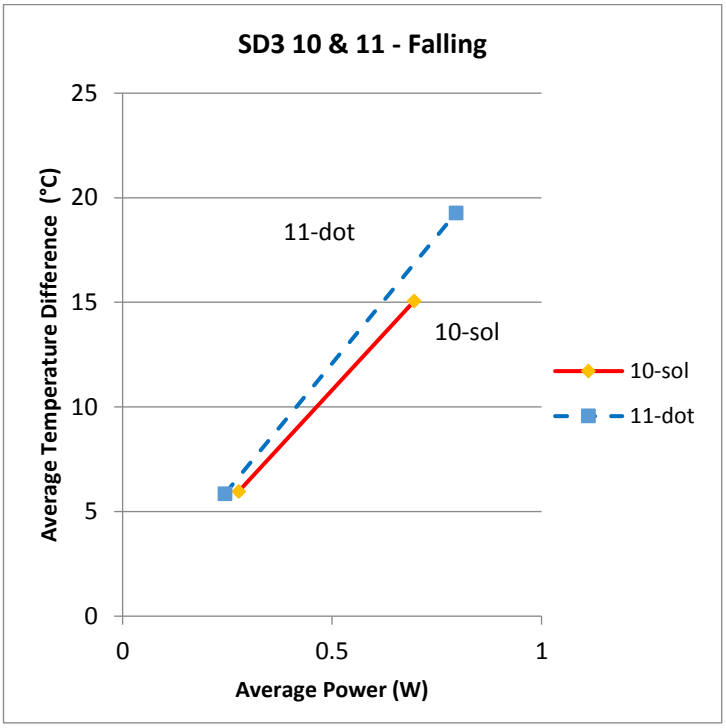

Figure 9-21 - SD3 10 & 11 Falling temperatures graph

Figure 9-22 - SD3 14 & 15 Rising temperatures graph

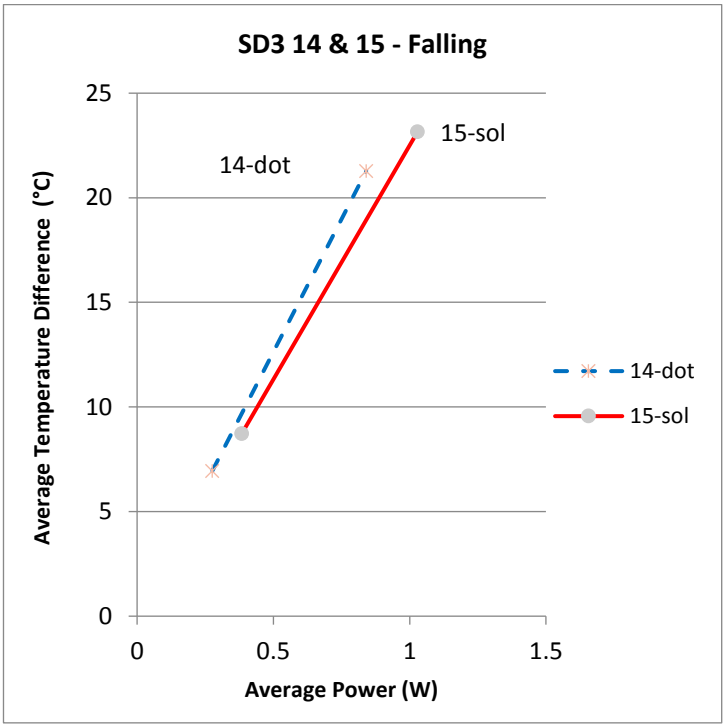

Figure 9-23 - SD3 14 & 15 Falling temperatures graph

9.7.3 **SD4 Substrate**

Below are the temperature graphs obtained for SD4 diodes 2,3,6,7,10,11,14 & 15.

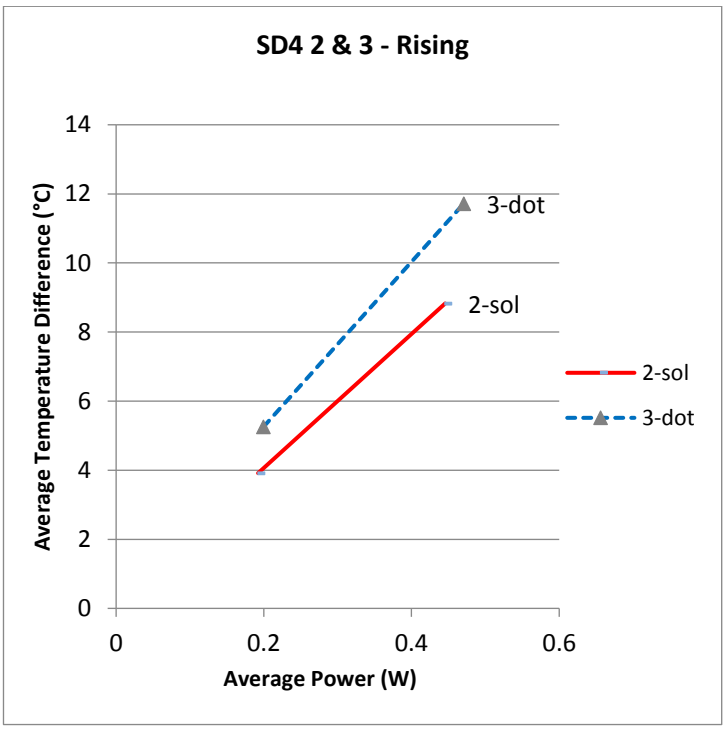

Figure 9-24 - SD4 2 & 3 Rising temperatures graph

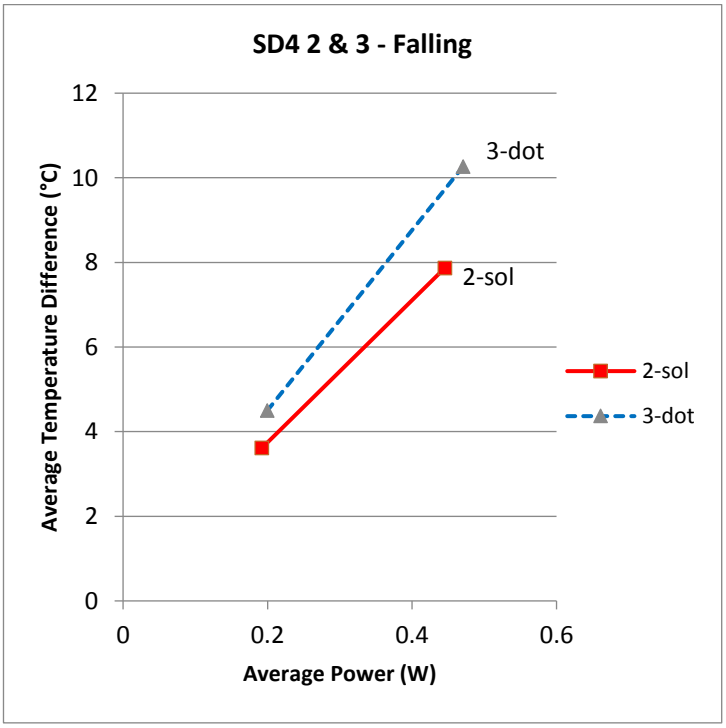

Figure 9-25 - SD4 2 & 3 Falling temperatures graph

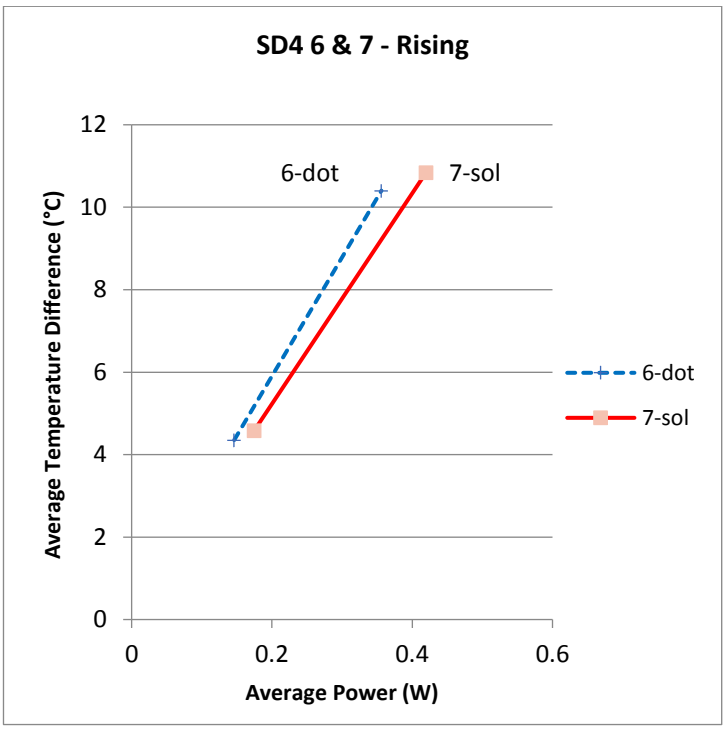

Figure 9-26 - SD4 6 & 7 Rising temperatures graph

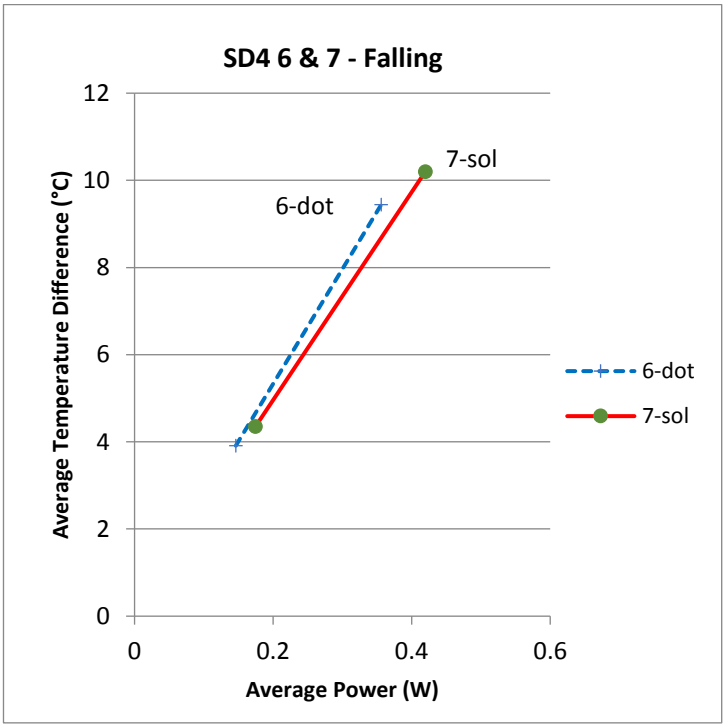

Figure 9-27 - SD4 6 & 7 Falling temperatures graph

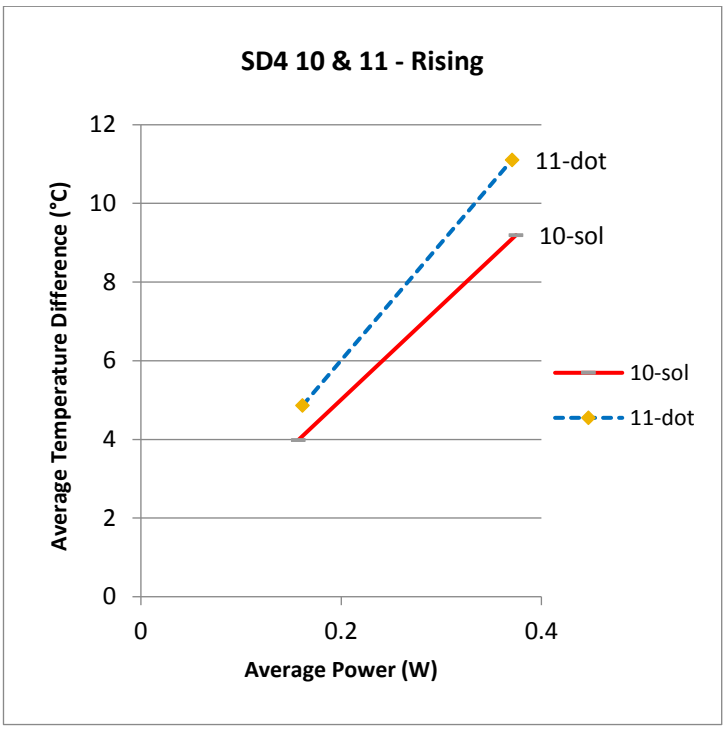

Figure 9-28 - SD4 10 & 11 Rising temperatures graph

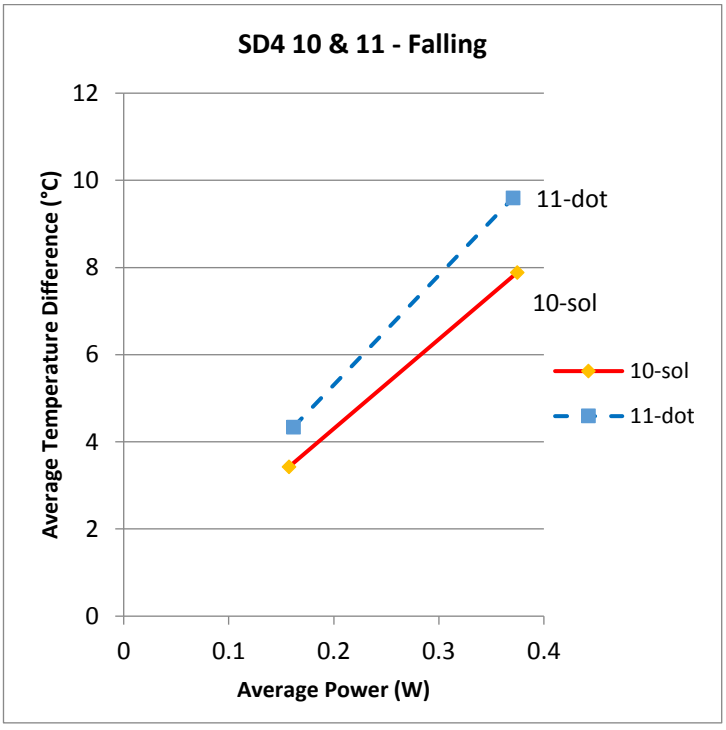

Figure 9-29 - SD4 10 & 11 Falling temperatures graph

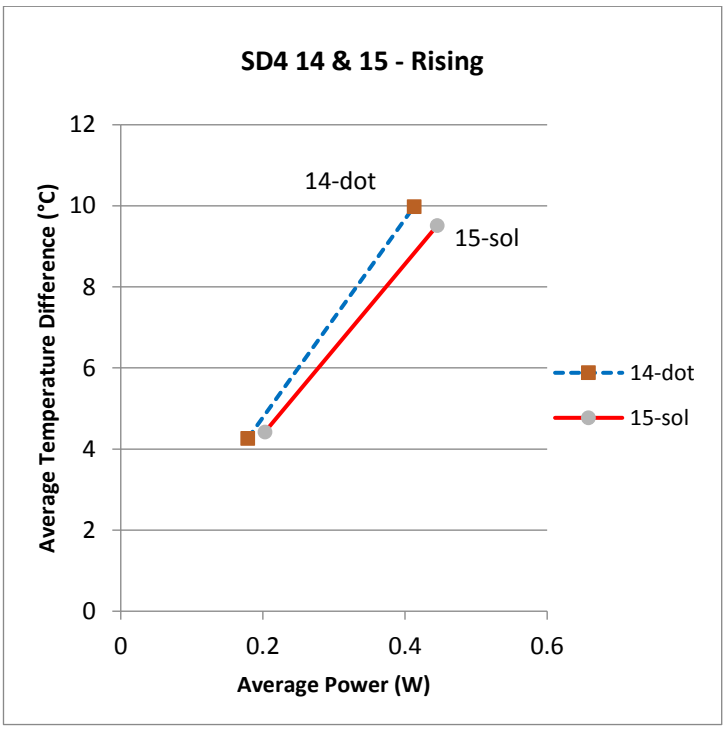

Figure 9-30 - SD4 14 & 15 Rising temperatures graph

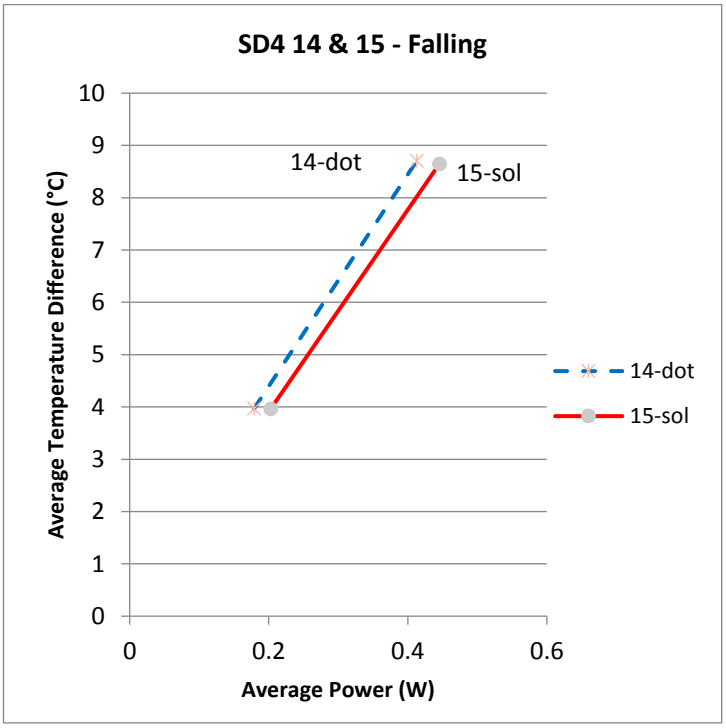

Figure 9-31 - SD4 14 & 15 Falling temperatures graph

9.7.4 **SD6 Substrate**

Below are the temperature graphs obtained for SD6 diodes 2,3,6,7,10 & 11.

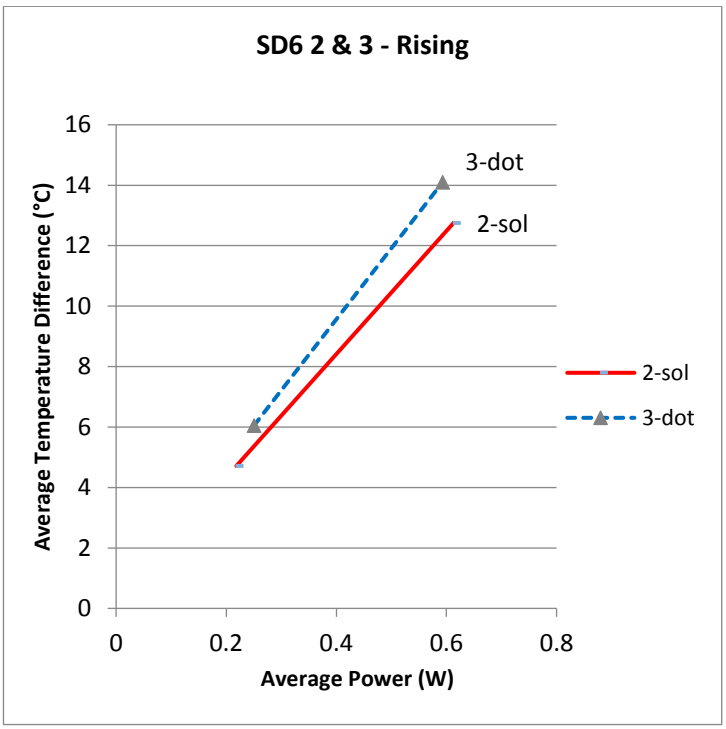

Figure 9-32 - SD6 2 & 3 Rising temperatures graph

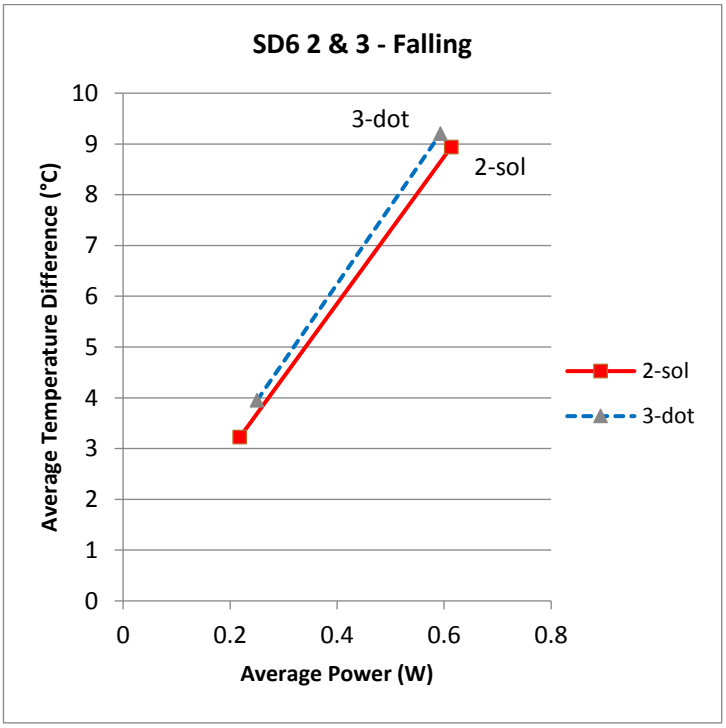

Figure 9-33 - SD6 2 & 3 Falling temperatures graph

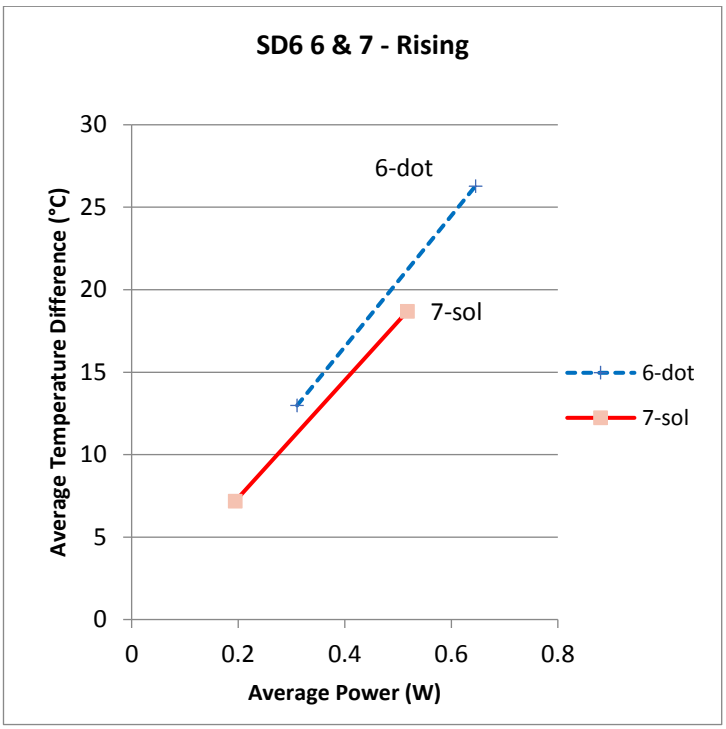

Figure 9-34 - SD6 6 & 7 Rising temperatures graph

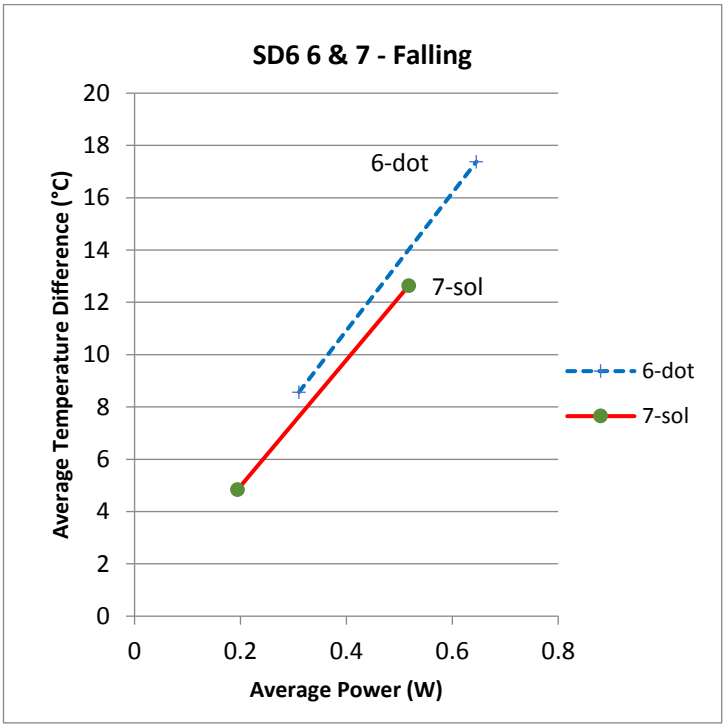

Figure 9-35 - SD6 6 & 7 Falling temperatures graph

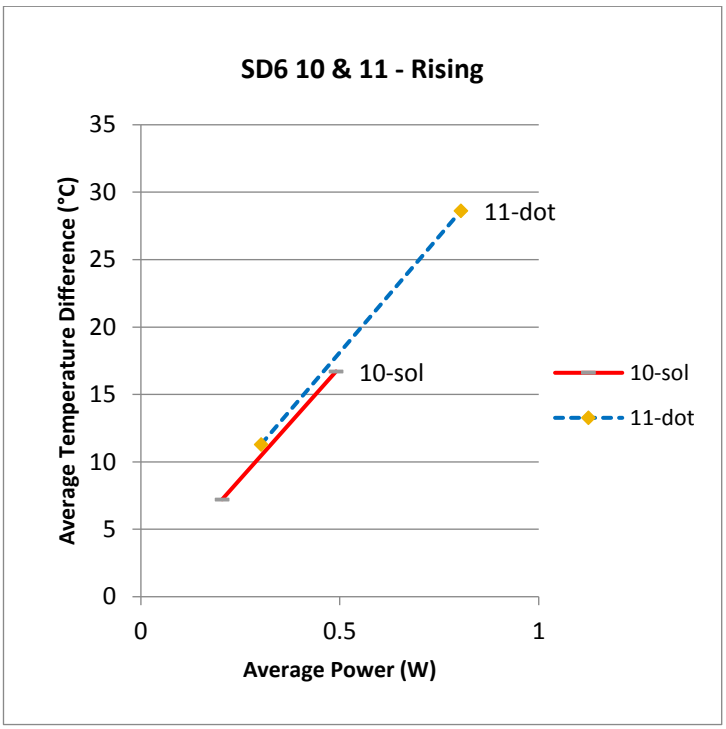

Figure 9-36 - SD6 10 & 11 Rising temperatures graph

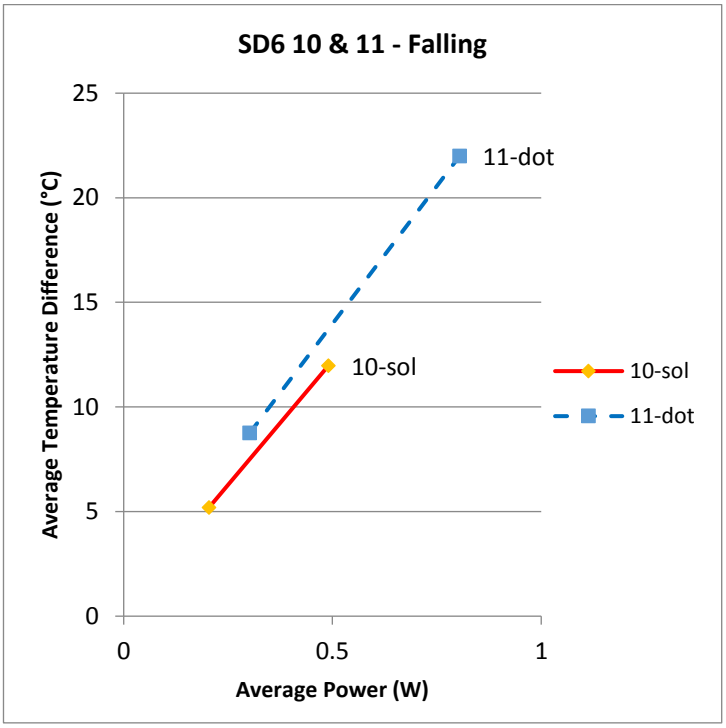

Figure 9-37 - SD6 10 & 11 Falling temperatures graph

9.7.5 **SD7 Substrate**

Below are the temperature graphs obtained for SD7 diodes 10,11,14 & 15.

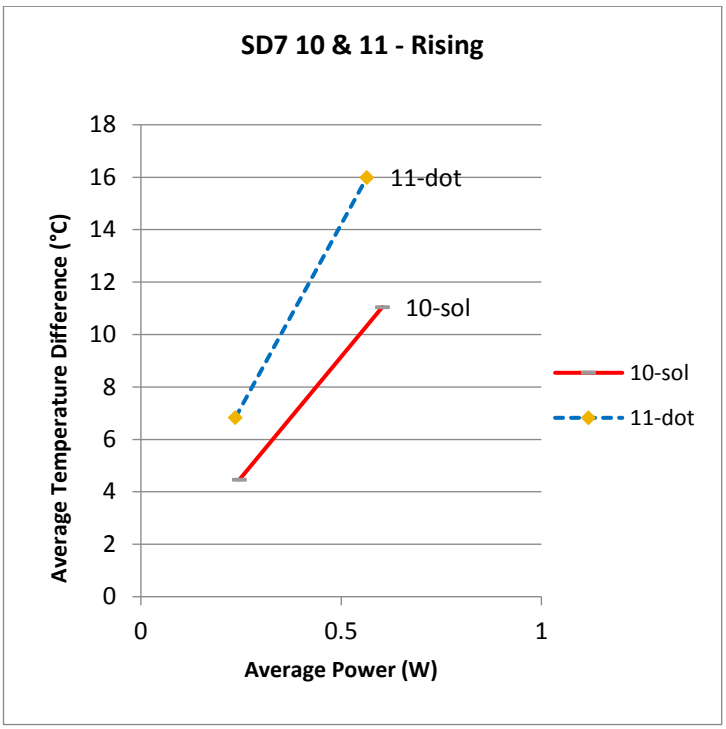

Figure 9-38 - SD7 10 & 11 Rising temperatures graph

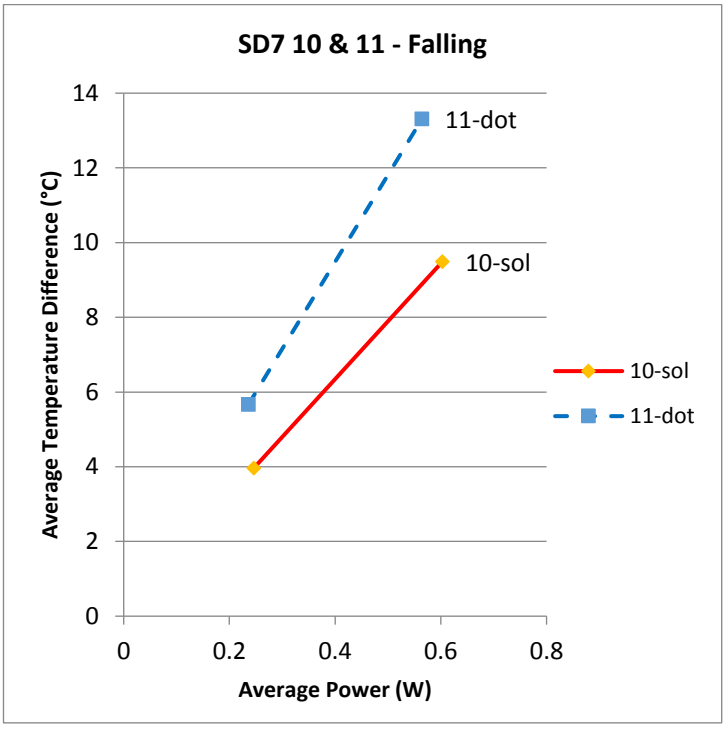

Figure 9-39 - SD7 10 & 11 Falling temperatures graph

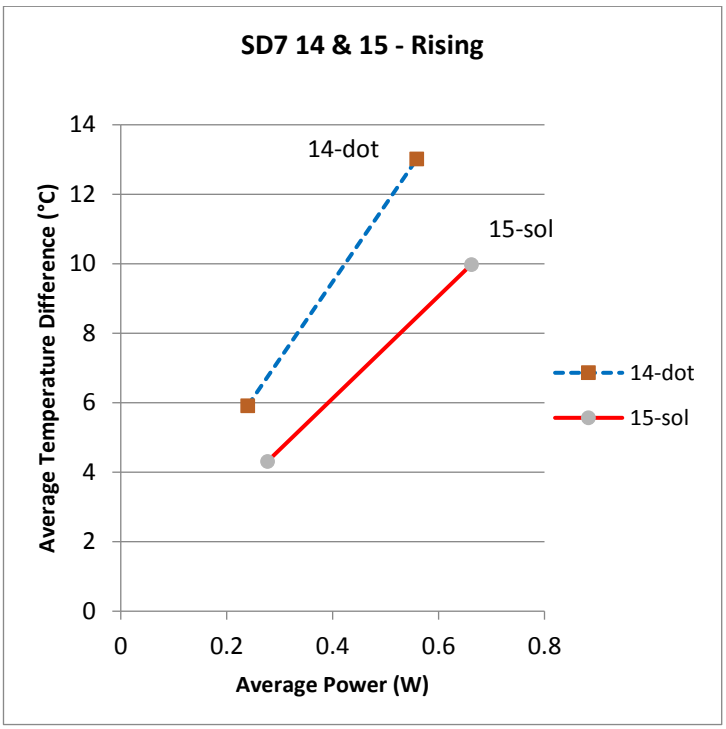

Figure 9-40 - SD7 14 & 15 Rising temperatures graph

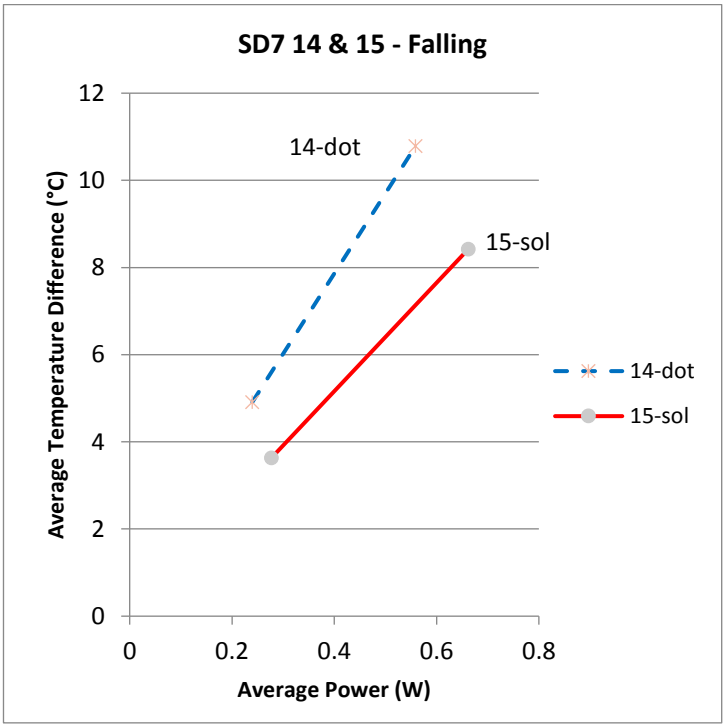

Figure 9-41 - SD7 14 & 15 Falling temperatures graph

9.7.6 **Block diode temperature summary**

The diodes which have been made out of pillars, have temperatures which rise and fall quicker than the ones made from a solid. This correlates well with the transient heat conduction theory as shown in

Figure 2-7 of chapter 2, where it has been shown that structures with a higher surface area to volume ratio, will heat up and cool down faster than an equivalent structure with the same volume, but a lower surface area to volume ratio. In addition, although no results have been obtained it can be implied, as discussed in chapter 2, that the operating temperature and the surface temperature of a device made with a higher surface area to volume ratio will operate cooler. This demonstrates that the didoes with the higher surface area to volume ratio can dissipate heat better, and as such waste less energy due to heat build-up, and are therefore more energy efficient.

The temperature graphs above are all in agreement, that the pillar diodes heat up and cool down faster. However, there is a difference between the blocks, and this has been accredited to the physical size of the blocks. The size of the blocks has been measured by hand with a ruler, and the volume of each of the blocks calculated using the measured length and width of the blocks, and the average etch depth taken away from the substrate thickness of approximately 500µm. This data is presented in Table 9-19 below.

Block	Av. etch Depth (m)	Diode	L (m)	W (m)	Height (m)	Volume (m^3)
SD2	3.45E-06	2 & 3				
		6 & 7	0.011	0.007	4.97E-04	3.82E-08
		10 & 11	0.011	0.007	4.97E-04	3.82E-08
		14 & 15				
SD3	3.27E-06	2 & 3	0.009	0.008	4.97E-04	3.58E-08
		6 & 7	0.009	0.005	4.97E-04	2.24E-08
		10 & 11	0.009	0.006	4.97E-04	2.68E-08
		14 & 15	0.009	0.006	4.97E-04	2.68E-08
SD4	3.40E-06	2 & 3	0.010	0.008	4.97E-04	3.97E-08
		6 & 7	0.010	0.004	4.97E-04	1.99E-08
		10 & 11	0.010	0.006	4.97E-04	2.98E-08
		14 & 15	0.010	0.008	4.97E-04	3.97E-08
SD6	3.29E-06	2 & 3	0.010	0.01	4.97E-04	4.97E-08
		6 & 7	0.010	0.004	4.97E-04	1.99E-08
		10 & 11	0.010	0.005	4.97E-04	2.48E-08
		14 & 15				
SD7	3.07E-06	2 & 3				
		6 & 7				
		10 & 11	0.01	0.005	4.97E-04	2.48E-08
		14 & 15	0.01	0.008	4.97E-04	3.98E-08

Table 9-19 - SD2/3/4/6 & 7 Block sizes and volumes

The volume data from Table 9-19 above has been plotted against the average temperature for each of the blocks extrapolated at 0.5W of power, the average temperature being the extrapolated temperature of the pillar and block diodes on the same block at 0.5W, and then the average taken of these two readings, Figure 9-42 below shows the graph.

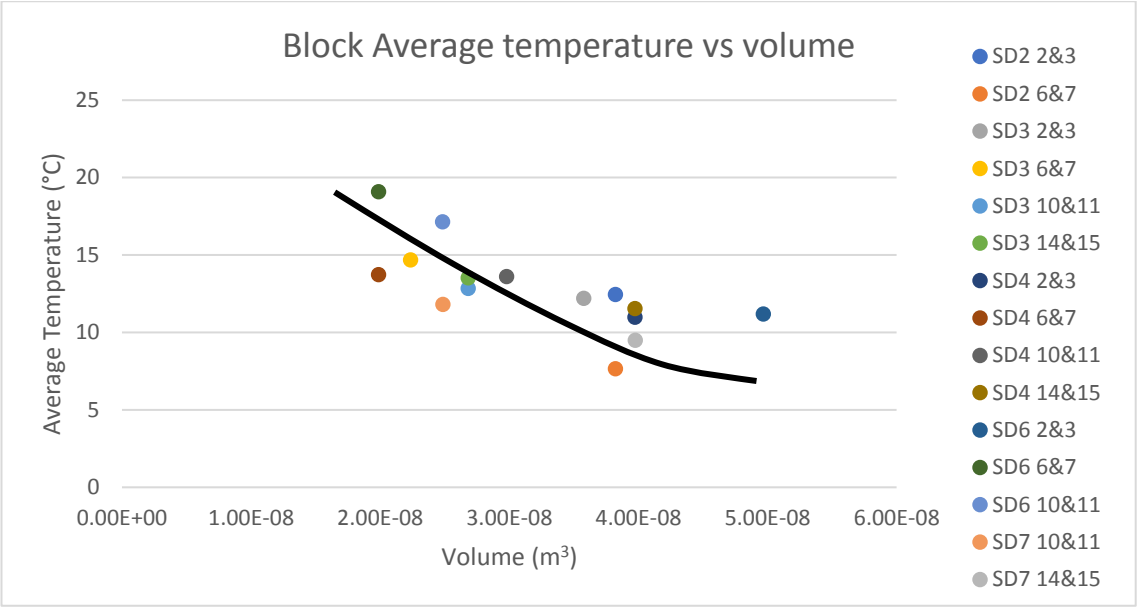

Figure 9-42 - SD2/3/4/6/7 Blocks average temperature vs volume

From the trend line on the graph it can be seen that although there is a small difference in the volume of the blocks, this does have an impact on the temperatures obtained.

The temperature graphs also show that the difference between the pillar and the solid diodes is not always the same. This may be due to the electrical characteristics i.e. the ideality factor. Figure 9-43 below shows a graph of the difference in ideality factor vs difference in temperature for the two diodes on each block, again the temperature has been extrapolated for 0.5W for each diode. There does appear to be a general trend where the larger the difference in ideality factor of the pillar, compared to the solid diodes, the greater the temperature difference. However, there are a few outliers which don't fit the trend. The ideality factor does look like it may have an impact on the temperature readings obtained, and hence why it appears the difference is not always the same.

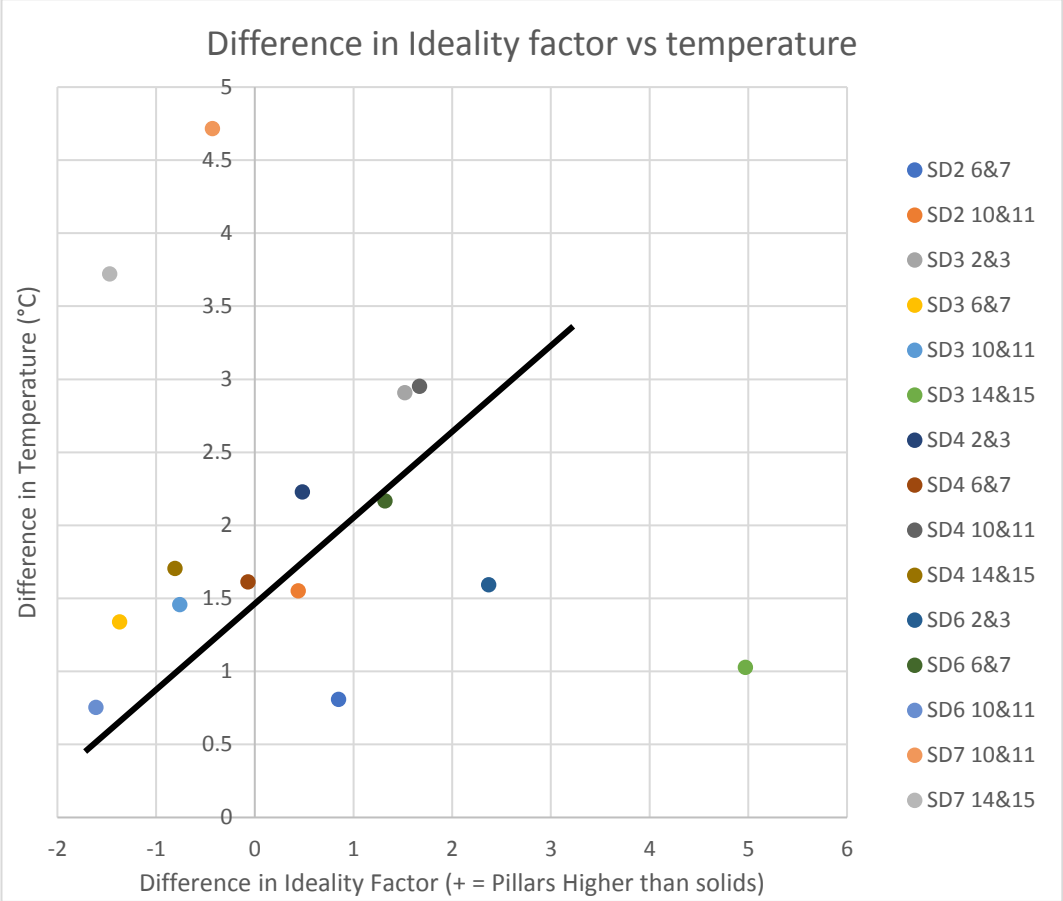

Figure 9-43 - SD2/3/4/6 & 7 Difference in Ideality factor vs temperature graph

Chapter 10 **Conclusion and future work**

10.1 Conclusion

At the onset of this research the intention was to make Schottky diodes from Si nanowires. However, the growing of vertical nanowires has been problematic, and it was looking like this would not be possible in time for my research. Because of this another method has been devised, to enable the construction of pillar diodes from a top down etching method using CF_4 or KOH, so that comparisons between differently constructed devices could be made. However, etching this way does not lend itself to producing Nano scale structures, and structures of 50µm diameter have been produced, to prove the principle of a device with a higher surface area to volume ratio will dissipate heat quicker, and operate at a lower temperature.

Devices have successfully been made from pillar and solid construction, which have good electrical characteristics, for the comparison of the surface area to volume ratio, by way of measuring the surface temperature rate of temperature rise and fall. A method has been devised to measure and record the surface temperature rise and fall, on the application of a constant current to the diodes.

The results from the tests carried out, and the comparison of the two different types of devices, has shown that the devices which have been made from the pillar construction, have a faster rise and fall in temperature for an equivalent power dissipation through the device. This confirms that these devices will operate at a lower temperature, and hence be more energy efficient, due to a lower rise in current due to the lower temperature of the device.

10.2 Future Work

Further work could be carried out on producing some diodes, with better electrical characteristics, by refining the manufacturing process. At present there are a lot of steps that are required to produce these diodes, and this is leading to contamination of the devices, which is causing higher ideality factors.

The method of production of the devices on a common substrate is good for comparison purposes, since they have all been subjected to the same

manufacturing process at the same time, which allows for more consistent diodes with like for like characteristics to be produced. However, as detailed in this thesis the size / volume of the substrate does have an effect on the temperature measurements, and a method of producing the diodes on a minimum size substrate would be advantageous.

To be able to have a finished Schottky diode, some form of in-fill is required between the pillars. This needs to be a material which is an insulator and has a high thermal conductivity, one such example of this would be Al oxide (Alumina) which has a thermal conductivity of 30 $Wm^{-1}K^{-1}$. A reliable method of applying this would need to be developed, as due to its high melting temperature this is difficult to evaporate, and would most likely need to be sputtered on to the surface, and a lift off process used to reveal the tops of the diodes, so that the top contact can be applied.

In addition, a good top Schottky contact needs to be applied. In this research it has been applied by evaporation, but has been shown with the SEM images this does not give a good overall coverage due to the method used. Dimaggio et al [64] has demonstrated a method of applying a reliable copper top contact on a forest of nanowires, but more work is required in this area still.

The research has demonstrated the principle of surface area to volume ratio on devices which are not of the Nano scale. More work will be required to be able to produce consistent nanowire forests, and then to apply the methods in this research to again demonstrate that this theory will hold fast. Having pillars of a smaller diameter, than those of this research, will provide better results due to the volume to surface area ratio being even higher.

Appendix 1 References

[1] *Freescale Semiconductor*. Thermal Analysis of Semiconductor Systems. White Paper 2008

[2] *Eric Pop*. Energy Dissipation and Transport in nanoscale Devices. Nano Research 3, 147 (2010)

[3] *Incropera. DeWitt, Bergman, Lavine*. Introduction to Heat transfer 5th edition. Wiley 2007 ISBN 0-471-45727-2.

[4] *Panasonic*. 3 Failure mechanism of Semiconductor Devices. T04007BE-2 2009.4

[5] *Williams B.W*. (1987). Cooling of power switching semiconductor devices. Power Electronics.

[6] *Wikipedia* – Allen's Rule. https://en.wikipedia.org/wiki/Allen%27s_rule

[7] *Gorazd Planinsic, Michael Vollmer*. The Surface-to-Volume ratio in thermal physics: from Cheese Cube Physics to Animal metabolism. Eur. J Phys 29 (2008) 369-384

[8] *R O Ocaya.* A current-voltage-temperature method for fast extraction of Schottky diode static parameters. Measurement 49 (2014) 246-255

[9] *Sachindra Nath Das, Jyoti Prakash Kar, Jae-Min Myoung*. Junction Properties and Applications of ZnO Single Nanowire Based Schottky Diode. Nanowires fundamental research Chapter 8.

[10] *S. Noor Mohammad*. Contact mechanisms and design principles for (Schottky and Ohmic) metal contacts to semiconductor nanowires. Journal of Applied Physics, v 108, n 3, August 1, 2010.

[11] *G S Chung, K S Kim, F Yakuphanoglu.* Electrical characterisation of AU/3C-SiC/n-Si/Al Schottky Junction. Journal of Alloys and Compounds 507 (2010) 508-512.

[12] *O Faruk Yuksel*. Temperature dependence of current-voltage characteristics of Al/p-Si (100) Schottky barrier diodes. Physica B 404 (2009) 1993-1997.

[13] *Ting-Fu Chang, Chih-Fang Huang, Tsung-Yu Yang, Chien-Wei Chiu, Tsung-Yi Huang, Jung-Yen Lee, Geng Zhao*. Low turn-on voltage dual metal AlGaN/GaN Schottky barrier diode. Solid-State Electronics 105 (2015) 12-15.

[14] *Mohan, Undeland, Robbins*. Power Electronics, john Wiley & Sons Inc, third edition 2003.

[15] S*.M. SZE, KWOK K. NG*. Physics of Semiconductor Devices. Wiley Third Edition 2007 ISBN 978-0-471-14323-9.

[16] *Yingying Li, Xiang Dong, Chuanwei Cheng, Xuechao Zhou, Peigen Zhang, Junshan Gao, Haiqian* Zhang Fabrication of ZnO nanorod array-based photodetector with high sensitivity to ultraviolet. (2009) Physica B: Condensed Matter, 404 (21), pp. 4282-4285.

[17] *Yi, G.-C., Yoo. J., Park, W.I., Jung, S.W., An, S.J., Kim, H.J., Kim, D.W*. ZnO nanorods for electronic and photonic device applications. (2005) Proceedings of SPIE - The international Society for Optical Engineering, 6003, art. No. 600301.

[18] *Sayan Bayan, Dambarudhar Mohanta*. Defect mediated optical emission of randomly orientated ZnO nanorods and unusual rectifying behaviour of Schottky nanojunctions. (2011) Journal of Applied Physics, 110 (5), art. No. 054316,.

[19] *L P Hackett, M A Seyedi, M Fiorentino, R G Beausoleil*. Large-area Silicon Nanowires Schottky Junction Photodetector with tunable Absorption and Low Junction Capacitance. J Phys D: Apply. Phys. 50(2017) 215105 (9pp).

[20] *J Yu, S J Ippolito, W Wlodarski, M Strano, K Kalantar-Zadeh.* Nanorod based Schottky contact gas sensors in reversed bias condition. (2010) Nanotechnology, 21 (16), art. No. 265502

[21] *Jisun Baek, Byungjin Jang, Min Hyung Kim, Wonkung Kim, Jeongmin Kim, Hyun Jun Rim, Sera Shin, Taeyoon Lee, Sungmee Cho, Wooyoung Lee*. High-Performance Hydrogen Sensing properties and Sensing mechanism in Pd-coated p-type Si nanowire arrays. Sensors and Actuators b 256 (2018) 465-471.

[22] *Goutam Chintakula, Suresh Rajaputra, Vijay P. Singh*. Schottky diodes on nanowires of copper phthalocyanine. Solar Energy Materials and Solar Cells, v 94, n 1, 34-9, Jan. 2010.

[23] *Peng Yu, Jiang Wu, Shenting Liu, Jie Xiong, Chennupati Jagadish, Zhiming M. Wang*. Design and fabrication of Silicon Nanowires towards efficient solar cells.

[24] *M.N. Jung, S.J. Oh, J.E. Koo, S.N. Yi, B.W. Lee, W.J. Lee, D.C. Oh, T. Yao, J.H.Chang.* One-step formation of ZnO nanorod bridge structure using geminated Si substrates by vapor phase Transportation. (2009) Current Applied Physics, 9 (2 SUPPL.), pp. e161-e164

[25] *Y.W. Heo, L.C. Tien, D.P. Norton, S.J. Pearton, B.S. Kang, F. Ren, J.R. LaRoche*. Pt/ZnO nanowire Schottky diodes. Applied Physics Letters Volume 85 Number 15 (11/10/2004).

[26] *W.I. Park, Gyu-Chul Yi, J.-W Kim, S.-M Park*. Schottky nanocontacts on ZnO nanorod arrays. (2003) Applied Physics Letters, 82 (24), pp. 4358-4360.

[27] *L.S. Chuah, Z. Hassan, S.S. Tneh, S.G. Teo*. Study of electrical Characteristics of ZnO Schottky photodiode on Si substrate. (2011) Microelectronics International, 28 (1), pp. 8-11

[28] *N. Bano, I. Hussain, O. Nur, M. Willander, H.S. Kwack, D. Le Si Dang*. Study of Au/Zno nanorods Schottky light-emitting diodes grown by low-temperature aqueous chemical method. (2010) Applied Physics A: Materials Science and Processing, 100 (2), pp. 467-472

[29] *Chu-Yeu, Peter Yang, Liwei Lin*. Vertical integration of ZnO nanowires into asymmetric Pt/ZnO/Ti Schottky UV photodiodes. 2011 IEEE 24th International Conference on Micro Electro Mechanical Systems (MEMS 2011), 1382-5, 2011

[30] *Parijat Deb, Hogyoung Kim, Yexian Qin, Roya Lahiji, Mark Oliver, Ronald Reifenberger, Timothy Sands.* GaN nanorod Schottky and p-n junction diodes. (2006) Nano Letters, 6 (12), pp. 2893-2898.

[31] *Chin-Jen Chiang. T.Mitch Wallis, Dazhen Gu. Atif Imtiaz, Pavel Kabos, Paul T. Blanchard, Kristine A. Bertness, Norman A. Sanford, Kichul Kim, Dejan Filipovic.* High frequency characterization of a Schottky contact to a GaN nanowire bundle. Journal of Applied Physics 107, 124301 (2010).

[32] *Seung-Yong Lee, Chan-Oh Jang, Jung-Hwan Hyung, Tae-Hong Kim, Sang-Kwon Lee*. High-Temperature characteristics of GaN nano-Schottky diodes. (2008) Physica E: Low-Dimensional Systems and Nanostructures, 40 (120), pp. 3092-3096.

[33] *Tae Il Lee, Won Jin Choi, Jyoti Prakash Kar, Youn Hee Kang, Joo Hee Jeon, Jee Ho Park, Youn Sang Kim, Hong Koo Baik, Jae Min Myoung*. Electrical Contact Tunable Direct Printing Route for a ZnO Nanowire Schottky Diode. Nano Letters; Sep2010, Vol. 10 Issue 9, p3517-3523, 7p

[34] *Sai Guduru, Vijay P. Singh, Suresh Rajaputra, Shounak Mishra, Raghu Mangu, Ingrid ST Omer*. Characteristics of gold/cadmium sulfide nanowire Schottky diodes. Thin Solid Films 518 (2010) 1809-1814.

[35] *E. Latu-Romain, P. Gilet, G. Feuillet, P. Noel, J. Garcia, F. Lévy, A. Chelnokov*. Optical and electrical characterizations of vertically integrated ZnO nanowires. Microelectronics Journal, Volume 40 Issue 2.

[36] *Walter Water, Te-Hua Fang, Yu-Jen Hsiao, Liang-Wen Ji, Ju-Hsuan Tsai, Ching-Chin Lee.* Structural, electromechanical and optical Characterisation of ZnO nanorods. (2011) Nanoscience and Nanotechnology Letters, 3 (4). Pp. 468-471.

[37] *Park, W.I., Yoo, J., Kim, H-J., Lee, C.H., Yi, G-C.* ZnO nanorods for electronic nanodevice applications. (2006) Proceedings of SPIE - The international Society for Optical Engineering, 6122, art. No. 612206.

[38] *P Klason, O Nur, M Willander.* Electrical Characteristics and stability of gold and palladium Schottky contacts on ZnO nanorods. (2008) Nanotechnology, 19 (47), art. No. 475202.

[39] *Park, W.I., Kim, D.-W., Jung, S.W., Yi , G.-C*. Catalyst-free growth of ZnO nanorods and their nanodevice applications. (2006) International Journal of Nanotechnology, 3 (2-3), pp. 372-395.

[40] *Ahmet Kaya. K. Gurkan Polat. Ahmed S. Mayet, Howard mao, Semsettin Altindal, M. Saif Islam*. Manufacturing and electrical Characterisation of Al-doped ZnO-coated Silicon nanowires. Material Science in Semiconductor Processing 75 (2018) 124-129.

[41] *Seung-Yong Lee, Sang-Kwon Lee*. Current Transport mechanism in a Metal-GaN nanowire Schottky diode. Nanotechnology 18 (2007) 495701 (4pp).

[42] *Yi, G.-C., Park, W.I., Kim, H.-J., Lee, C,-H.* ZnO nanorods for electronic nanodevice applications. (2006) 2006 IEEE Nanotechnology Materials and devices Conference, NMDC, 1, art. No. 4388728, pp. 164-165.

[43] *Park, W.I., Kim, J.S., Yi, G.-C., Lee, H-J*. ZnO nanorod logic circuits. (2005) Advanced Materials, 17 (11), pp. 1393-1397.

[44] *Guo, Wei; Banerjee, Animesh; Zhang, Meng; Bhattacharya, Pallab*. Barrier height of Pt–$In_xGa_{1-x}N$ ($0 \leq x \leq 0.5$) nanowire Schottky diodes. *Applied Physics Letters* , vol.98, no.18, pp.183116-183116-3, May 2011

[45] *O. Kubo, Y. Shingaya, M. Aono, T. Nakayama*. One-dimensional Schottky contact between ErSi2 nanowire and Si(001). (2006) Applied Physics Letters, 88 (23), art. No. 233117.

[46] *Hafez. M., Al-Marzouki, F., Mahmoud, W.E*. Single crystaline quasi aligned one dimensional P-type Cu2O nanowire for improving Schottky barrier characteristics. (2011) Material Letters, 65 (120), pp. 1868-1870

[47] *Shao ZhengZheng, Zhang XueAo, Wang XiaoFeng, Chang ShengLi*. Electrical characteristics of Pt-ZnO Schottky nano-contact. (2010) Science China: Physics, Mechanics and Astronomy, 53 (1), pp. 64-67

[48] *J Piscatora, O Engstrom*. Schottky Barriers on Silicon Nanowires Influenced by Charge Configuration. Journal of Applied Physics 104, 054515 (2008).

[49] *Piao Liu, Vijay P. Singh, Suresh Rajaputra, Sovannary Phok, Zhi Chen.* Characteristics of copper indium dieseline nanowires embedded in porous alumina templates. Journal of Materials Research, v 25, n 2, p 207-212, February 2010.

[50] *A El Sachet, J S Reparaz, J Spiece, M L Alonso, A R Goni, M Garriga, P O Vaccaro, MR Wagner, O V Kolosov, C M Sotomayor Torres, F Alzina*. Thermal Transport in Epitaxial $Si_{1-x}Ge_x$ alloy nanowires with varying composition and Morphology

[51] *Eric Pop, Kenneth E Goodson*. Thermal Phenomena in Nanoscale Transistors. Stanford University

[52] *Eric Pop, Kenneth e Goodson*. Thermal Phenomena in Nanoscale Transistors. IEEE Vol. 128, June 2006

[53] *Warefta Hasan, Christopher L Stender, Min Hyung Lee, Colleen L Nehl, Jeunghoon Lee, Trei W Odom*. Tailoring the Structure of nanopyramids for Optimal Heat Generation. Nano Lett 2009 April 9(4) 1555-1558.

[54] *Yougshun Sun, Rusli, Hong Wang, Kai Lin Foo, Wen Xu*. Silicon-nanowire-based Schottky diode with near-ideal breakdown voltage. (2010) IEEE Electron Device Letters, 31 (11), art. No. 5567130, pp. 1187-1189

[55] *Ning Zhang, Ke Yu, Lijun Li, Ziqiang Zhu*. Investigation of electrical and ammonia sensing characteristics of Schottky barrier diode based on a single ultra-long ZnO nanorod. (2008) Applied Surface Science, 254 (18), pp. 5736-5740.

[56] *Z.Y. Zhang, C.H. Jin, X.L. Liang, Q Chen, L.-M. Peng*. Current-voltage Characteristics and parameter retrieval of semiconducting nanowires. Applied Physics Letters, v 88, n 7, 73102-1-3, 13 Feb. 2006

[57] *Chanoh Hwang, Jung-Hwan Hyung, Seung-Yong Lee, Chan-Oh Jang, Tae-Hong Kim, Pyung Choi, Sang-Kw Lee*. The formation and characterisation of electrical contacts (Schottky and Ohmic) on gallium nitride nanowires. Journal of Physics D: Applied Physics, v 41, n 10, May 21, 2008.

[58] *Yong Lin, Qiming Li, Andrew Armstrong, George T. Wang*. In situ scanning electron microscope electrical characterisation of GaN nanowire nanodiodes using tungsten and tungsten/gallium nanoprobes. Solid State Communications, v 149, n 39-40, p 1608-1610, October 2009.

[59] *Jae-Ryoung Kim, Hwangyou Oh, Hye Mi So, Ju-Jin Kim, Jinhee Kim, Cheol Jin Lee, Seung Chul Lyu.* Schottky diodes based on a single GaN nanowire. Nanotechnology, 13 (2002) 701-704.

[60] *Das, S.N.1; Kar, J.P.1; Choi, J.H.1; Moon, K.J.1; Lee, T.I.1; Myoung, J.M*. Electrical characterisation of single nanowire based ZnO Schottky diodes. 2010 IEEE 3rd International Nanoelectronics Conference (INEC 2010).

[61] *S.n. Das, J.P. Kar, J.H. Choi, K.J. Moon, T.I. Lee, J.M. Myoung*. Electrical Characterisation of single nanowire based ZnO Schottky Diodes. IEEE 2010.

[62] *Wen-Chung Chang, Sheng-Chien Su, Chia-Ching Wu*. The development of high-density vertical silicon nanowires and their application in a Heterojuction Diode. Materials 2016, 9, 534.

[63] *Gourab Sabui, Vitaly Z. Zubialevich, Mary White, Pietro Pampili, Peter J. Parbrook, Mathew McLaren, Miryam Arredondo-Arechavala, Z. John Shen.* GaN Nanowire Schottky Barrier Diodes. IEE Transactions on Electron Devices, Vol 64, No. 5 May 2017.

[64] *Elisabetta Dimaggio, Giovanni Pennelli.* Reliable Fabrication of Metal Contacts on Silicon Nanowire Forests. Nano Letters 2016, 16, 4348-4354.

[65] *Sang-Won Jee, Joondong Kim, Jin-Young Jung, Han-Don Um, Moiz Syed Abdul, Bongyoung Yoo, Hyung Koun Cho, Yun Chang Park, Jung-Ho Lee*. Ni-catalyzed growth of silicon wire arrays for a Schottky diode. Applied Physics Letters; 7/26/2010, Vol. 97 Issue 4, p042103, 3p, 3 Diagrams, 1 Graph

[66] *Sheu, J.T., Yeh, S.P., Lien, C.H., Tsai, S.T*. Fabrication and electrical characterization of nanoscaled-schottky diodes based on metal silicide/silicon nanowires with scanning probe lithography and wet etching. (2006) Japanese

Journal of Applied Physics, Part 1: Regular Papers and Short Notes Review Papers, 45(4B), pp. 3686-3689.

[67] *C Y Ho, S H Chiu, J J Ke, K T Tsai, Y A Dai, J H Hsu, M L Chang, J H He*. Contact behaviour of focused ion Beam Deposited Pt on p-type Si Nanowires. Nanotechnology 21 (2010) 134008 (5pp)

[68] *Alfred Grill*. Cold Plasma in Material Fabrication. IEEE Press 1994.

[69] *Kirt R Williams.* Etch Rates for Micromachining Processing – Part II. Journal of Microelectromechanical Systems Vol 12 No. 5 December 2003.

[70] *Tina J. Cotler, Michael E. Elta.* Plasma-Etch technology. IEEE July 1990.

[71] *M. M. Yovanovich, J.R. Culham, T.F. Lemczyk*. Simplified Solutions to circular annular Fins with contact resistance and end cooling. J. Thermophysics Vol 2 No. 2.

[72] *Hong-Sen Kou, JI-Jen Lee, Chi-Yuan Lai*. Thermal Analysis and optimum Fin Length of a heat sink. Heat transfer engineering, 24(2): 18-29, 2003.

[73] *Siva Uppuluri.* Understanding Semiconductor thermal resistance data. Diodes incorporated 2016.

[74] 1N5817 Schottky Diode data sheet, ON Semiconductor, RS Part Number 625-4972

[75] SB120 Schottky Diode data sheet, Fairchild, RS Part Number 806-1980

[76] MBR1100 Schottky Diode data sheet, RS Part Number 781-5629

[77] *Dieter K. Schroder*, "Optical Characterization," in *Semiconductor Material and Device Characterization* , , IEEE, 2006, pp. doi: 10.1002/0471749095.ch10

[78] *Thomas Attia Mih.* PhD 2011 De Montfort University.

[79] *M. Watt Ian*., *The principles and practice of electron microscopy,* Cambridge University Press, 1985.

[80] *A.M. Efremov, Dong-Pyo Kim, Chang-Il Kim.* Effect of gas mixing ratio on gas-phase composition and etch rate in an inductively coupled CF_4/Ar plasma. Vacuum 75 (2004) 133-142.

[81] *S J Chang, Y Z Juang, D K Nayak, Y Shiraki.* Reactive ion etching of Si/SiGe in CF_4/Ar and Cl2/BCl3/Ar discharges. Materials Chemistry and Physics 60 (1999) 22-27.

[82] *Henri Jansen, Han Gardeniers, Meint de Boer, Miko Elwenspoek, Jan Fluitman.* A survey on the reactive ion etching of silicon in microtechnology. J Micromech Microeng 6 (1996) 14-28.

[83] *Siti Azlina Rosli, Azlan Abdul Aziz, Haslinda Abdul Hamid*. Highly chemical reactive Ion etching of silicon in CF_4 containing plasmas. ISCE2006 Proc 2006.

[84] *Mahla Poudineh, Zeinab Sanaee, Azam Gholizadeh, Samaneh Soleimani, Shamsoddin Mohajerzadeh*. Formation of highly ordered silicon nanowires by high-speed deep etching. IEE Transactions on Nanotechnology, Vol. 12, No. 5. 2013.

[85] *S K Ray, C K Maiti, N B Chakraborti*. Rapid plasma etching of Silicon, Silicon dioxide and Silicon nitride using microwave discharges. Semicond. SCI. Technol. 8 (1993) 599-604.

[86] *O V Balachova, M A R Alves, J W Swart, E S Braga, L Cescato*. CF_4 plasma etching of materials used in microelectronics manufacturing. Microelectronics Journal 31 (2000) 213-215.

[87] *Marco A R Alves, Olga balachova, Edmundo da Silva Braga, Lucila Cescato*. Selective deposition of amorphous hydrogenated carbon films used as masks for reactive ion etching of Si using CF_4. Vacuum 52 (1999) 313-314.

[88] *Robert J Moekstra, Mark J Kushner, Valeriy Sukharev, Phillipe Schoenborn.* Microtrenching resulting from specular reflection during chlorine etching of silicon. J VAN Sci Technol B 16(4) Jul/Aug 1998

[89] *K. Westra*. KOH and TMAH Etching of Bulk Silicon. February 11, 2010.

[90] *Norhafizah Burham, Azrul Azlan Hamazh (MIEE), Burhanuddin Yeop Majlis (SMIEE).* Effect of Isopropyl Alcohol (IPA) on Etching Rate and Surface Roughness of Silicon Etched in KOH Solution. IEEE 2015 978-1-4799-8550-0

[91] *Kirt R Williams, Richard S. Muller*. Etch Rates for Micromachining Processing. Journal of Microelectromechanical Systems Vol 4 No. 4 December 1996.

[92] *Tiago S. Monteiro, Pamakstys Kastytis, Luis M. Goncalves, Graca Minas and Susana Cardoso.* Dynamic Wet Etching of Silicon Through Isopropanol Alcohol Evaporation. Micromachines 2015, 6, 1534-1545

[93] *Kihyung Ko, Myung-Geun Song, Hayoung Jeon, Jungnam Han, Bo Un Yoon, Yongsun Koh, Chisung Ahn, Taesung Kim*. Characterisation and removal of polysilicon residue during wet etching. Microelectronic Engineering 1 49 (2016) 85-01

[94] www.lelandstanfordjunior.com

[95] www.cleanroom.byu.edu

[96] J Electrochem. Soc. Vol 137, 11, Nov 1990, 3612 – 3632

[97] *Tatsuya Enomoto, Masahiko Denda, A Kihiko Yasuoka and Hidefumi Nahata*. Loading effect and temperature Dependence of Etch rate in CF4 plasma. Japanese Journal of Applied Physics Vol. 18, No. q, January 1979 pp. 155-163.

[98] *Hiroto Ohtake, Tomiko Wanifuchi, Masaru Sasaki*. SiN etching characteristics of $Ar/CH_3F/O_2$ plasma and dependence on SiN film density. Japanese Journal of Applied Physics 55, 086502 (2016).

[99] *C. Reyes-betanzo, S.A. Moshkalyou, M.A. Pavanello, A.C.S. Ramos, J.W. Swart*. Plasma Etching of Si_3N_4 with High Selectivity Over Si and SiO_2. Centro de Components Semiconductors – CCS, UNICAMP, C.P. 6061, CEP. 13083-970, Campinas, SP, Brazil.

[100] *B.E.E/ Kastenmeier, P.J. Matsuo, J.J. Beulens, G.S. Oehrlein.* Chemical Dry Etching of Silicon Nitride and Silicon Dioxide Using $CF_4/O_2/N_2$ gas mixtures. J. Vac Sci. Technol. A 14(5) Sep/Oct 1996.

[101] *Ohring, Milton*. Materials Science of Thin Films, Elsevier Science & Technology, 2001. ProQuest Ebook Central

[102] *sigma Aldrich*. Technical Bulletin Negative Photoresist Kit. 2004.

[103] www.ossila.com

[104] *Irena Barycka, Irena Zubel.* Silicon Anisotropic etching in KOH-isopropanol etchant. Sensors and Actuators A 48 (1995) 229-238